NEW GENERATION THREE-PHASE RECTIFIER

By

William Phipps

A thesis presented for the degree of Doctor of Philosophy

In

Electrical and Electronic Engineering at the

University of Canterbury, Christchurch New Zealand

July 2008

TABLE OF CONTENTS

ABSTRACT

This thesis describes the development of a new generation of three-phase rectifier, used to power telecommunications equipment. The traditional topology for such power converters is a single-phase two-stage design, with a boost converter providing power factor correction at the input to the first stage and an isolated dc-dc converter making up the second stage. A two-stage design results in the output power being processed twice and this cascade effect results in an overall reduction in efficiency. A rectifier solution is sought that meets with all the requirements of the telecommunications industry, while not displaying the inherent weaknesses associated with a boost-derived topology, and which can be realised in a single-stage design. A number of common three-phase topologies exist that could be realised as telecommunication power supplies, however, they do not completely satisfy all the industry requirements. A new three-phase rectifier, which is a single-stage buck-derived topology, is proposed. As a consequence of incorporating a buck-derived topology, the three-phase rectifier does not exhibit any issues resulting from startup inrush currents, or high currents due to an output short circuit condition, as would result in a boost-derived topology. The new proposed rectifier is modular in nature, which has the added benefit of redundancy. As a result of the new three-phase rectifier having a single-stage topology, it is expected that the overall efficiency would able to reach close to 95%. This is due to the traditional two-stage designs having efficiencies around the 90% mark, and therefore by removing a stage, out of the power conversion process the overall losses would also be halved, resulting in the 5% gain in efficiency. The rectifier system requires only one controller as a result of being a single-stage design, thus also reducing the overall system cost.

Simulations show that if this topology is combined with a three-phase phase-locked loop controller it can meet the industry compliance standards. The thesis follows the development of the three-phase power converter from the simulation stage to the realisation of the control hardware and stability modelling. It also provides a detailed report of an investigation into the power converter system's performance. The thesis concludes with discussions concerning the viability of the new topology as a commercial product and indicates areas of possible future research and development.

ACKNOWLEDGEMENTS

I wish to take a moment to thank a number of people, without whom this work would not have been possible. Firstly, I would like to acknowledge my supervisor Richard Duke for the valuable guidance and input he has given me while undertaking this research work. I also wish to thank Michael Harrison for the sound technical advice and lateral thinking which make this project come together in the end. I would like to acknowledge the financial support from the TIF scholarship as well as the additional contributions from Easton Power Quality Ltd. I would also like to thank my wife Kaaren for her continued support and encouragement throughout the duration of this project. Above all, I thank the Lord for opening up the doors and created the opportunity for me to do this project and helping me to complete it.

1 INTRODUCTION

Telecommunication systems are designed primarily to provide the backbone infrastructure to facilitate communication. This includes using mediums such as telephone, internet and wireless systems. A telecommunication system is made up of various elements; these include telecommunication switching equipment, power supply cabinets, a standby battery system, a mains transfer switch and a standby generator. A typical telecommunication installation is shown in Fig. 1.1.

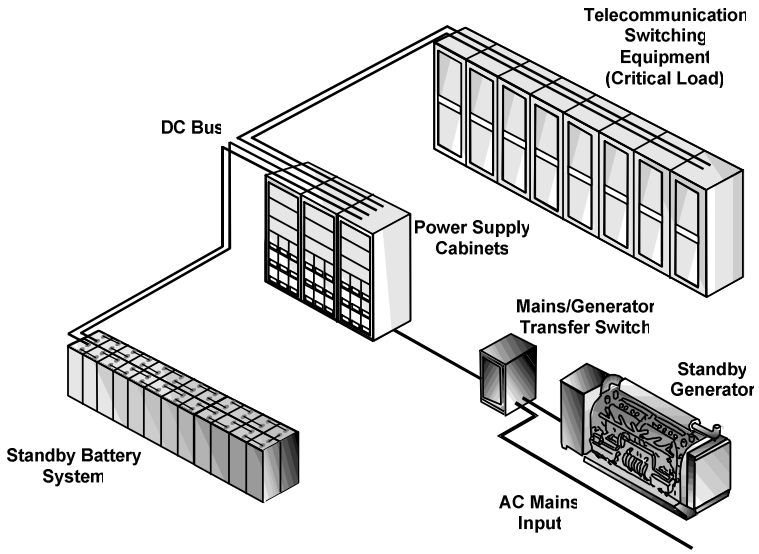


Fig. 1.1 Typical Telecommunication Installation

Typically a telecommunication system has the AC mains input as the primary power source for the installation, with some critical installations having an alternative supply in the form of a standby generator. In this case both the generator output and the AC mains input are routed to the power supply cabinets via a mains/generator transfer switch. In the event that the mains supply is compromised this switch is activated allowing the generator to supply energy to the system. During the generator start-up phase the standby batteries provide power to the telecommunication switching equipment.

Power converter systems which convert the AC mains voltage to a -48V DC supply are housed inside the power supply cabinets. These power converter systems are used to provide the batteries with charging current when necessary, as well as powering the telecommunication switching equipment, which mainly consists of board mounted power converter units used to convert the -48V to 5V and ±12V.

1.1 Telecommunication Industry Standards

Telecommunication power converter systems have to comply with various industry standards in order for manufacturers to be able to sell their products. Two standards which have a significant impact on the design of the power converters are described in the following two subsections.

1.1.1 ITU-T 0.41 (psophometric) Standard

The term psophometric is used to describe a method of measuring noise within the speech band, while weighting the value of each frequency component present in accordance with its relative effect on the human ear [1]. The psophometric standard was introduced by the International Telecommunications Union (ITU); its purpose is to regulate the amount of audible noise appearing on telephone networks. This was due to the fact that in the telecommunications industry Silicon Controlled Rectifier (SCR) full bridge converters were used before the introduction of switched mode technology into the market place. These SCR converters had no output filtering and as a result had considerable noise on the output due to the presence of lower order harmonics [2]. Telephone systems were originally analogue, and as a result of the lower order harmonics on the SCR converter output, audible noise was produced on the telephone lines. Reducing this audible noise was achieved by adding passive LC filtering components on the output of the SCR converters. However, this resulted in an increase in size and cost. Nowadays, with digital

exchanges, the telephone systems have become more immune to DC power supply noise. Since digital signals only exist in discrete states and not continuous signals, it is therefore only necessary to detect a high or low state on a digital signal. The psophometric standard is still used however as the defining standard for the interface between telecommunication switching equipment and telecommunication power converter systems, hence companies must meet the standard in order to sell their products. The psophometric noise limit is defined for telecommunication power converter systems such that the AC output voltage is not to exceed 2mVrms while the system is operating under full load at nominal mains voltages.

1.1.2 IEC 1000-3-2 Standard

The IEC1000-3-2 standard was introduced in 1995 to regulate harmonic currents drawn from the mains supply [3]. These harmonic currents reduce the supply efficiency and can excite resonances, as well as causing heating in transformers and wiring. Telecommunication power converter systems fall under a Class A classification which defines all electrical and electronic equipment having an input current up to and including 16A per phase. The Class A limits of harmonics for each phase of the line current are shown in Table 1. These limits are absolute, i.e. not related to power ratings of the equipment. The limits are only applicable to steady-state harmonic currents since harmonic distortion is a characteristic of the steady-state current or voltage and is not a disturbance [4].

Harmonic Order (n)	Maximum Harmonic Current (Amps)
Odd harmonics	
3	2.3
5	1.14
7	0.77
9	0.4
11	0.33
13	0.21
$15 \le n \le 39$	2.25/n
Even harmonics	
2	1.08
4	0.43
6	0.3
$8 \le n \le 40$	1.84/n

Table 1 Class A Harmonic Current Limits [IEC1000-3-2]

1.2 Standards Compliance

Compliance with these two standards has dictated the way in which telecommunication power converter system manufacturers have to design their products. The most popular choice is a single-phase two-stage topology [5-9] as shown in Fig. 1.2.

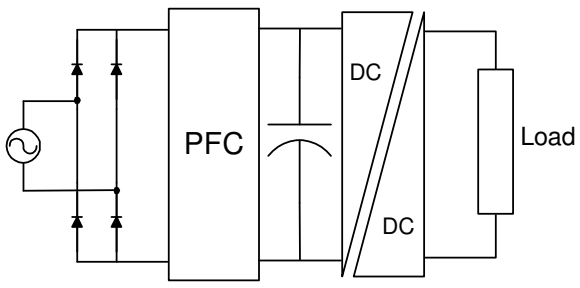


Fig. 1.2 Traditional Telecommunication Power Converter System

The first stage of the power converter system comprises a boost stage, used to provide power factor correction (PFC) and hence regulate the maximum allowable input harmonic current content defined by the IEC1000-3-2 standard [3, 10]. The simple boost converter topology is the most popular choice for a PFC stage, due to its high efficiency and good silicon utilization [11]. Traditional single-phase telecommunication power converter systems typically operate up to 6kW power range, with the cost of bulk storage capacitors becoming the limiting factor as well as the ability to draw larger amounts of power off one phase of a supply transformer.

Also, the boost stage requires that the output voltage selected is higher than the highest peak value of input voltage, which in a universal boost topology capable of operating on both 110V and 220V systems, typically results in an output voltage of 400V or more [12]. Since telecommunication switching equipment runs off a -48V supply, there is the additional need for voltage transformation. Also, telecommunication companies have chosen not to have isolation of their systems, and since the standby batteries have their positive 48V rail earthed it therefore becomes a functional requirement for the power converter system to have galvanic isolation. The second stage takes the form of a DC-DC converter which is required to provide fast regulation of the output voltage to reject the psophometric noise, as well as providing the isolation and voltage transformation.

As a consequence of having a single-phase supply no power can be transferred during the mains zero crossings; hence a large storage capacitor is needed to provide the output power during these times. As a result of having a two-stage topology there are losses across both stages as the power is processed twice, this results in a cascading effect which reduces the overall efficiency of the system, resulting in typically around 90% efficiency. Having a boost stage has the disadvantage that there is no protection from short circuit conditions and startup inrush currents [13]. Also, two separate

control circuits are required, one for each stage adding to the overall cost of the system. A further discussion into single-phase topologies is explored in the next chapter.

1.3 Project Motivation

The project was undertaken in collaboration with Eaton Power Quality Ltd., a company that specialises in producing telecommunication power converter systems. Increased competition in the marketplace has forced the company to re-evaluate its range of products. Since the power converter system contributes a significant part to the cost of the overall power supply solution, it became the logical focus of attention in the cost reduction drive. It was identified that in order to achieve a cost reduction in the power converter system, a reduction in the dollar per watt ratio was needed. One way of reducing the dollar per watt ratio is by increasing the overall power converter system efficiency. Since an increase in efficiency results in the power converter system size reduction for the same output power, this translates directly to a reduction in the cost of the componentry, hence a reduction in the dollar per watt ratio. A dollar per watt decrease leads to production cost savings which are passed on to the customer allowing for organic sales growth through a cost advantage in the market.

Eaton Power Quality Ltd. investigated various ways of increasing the efficiency of their single-phase two-stage power converter system. These included moving from the conventional powdered iron inductor cores to high frequency gapped ferrite cores; the use of Litz wire in both PFC and second stage magnetic components as well as using modern FETs and power diodes. By adopting these design methods they were able to improve their power converter system product efficiency to 92%. It then became apparent that any further increase in efficiency was not possible using their existing single-phase two-stage topology. Hence, the only way possible to obtain a further

increase in efficiency, as well as still meeting with the required industry standards, was to investigate suitable topologies other than the traditional single-phase two-stage approach.

1.4 Scope of Thesis

This thesis proposes a new three-phase power converter topology specifically designed to meet the telecommunication industry requirements as well as providing an increased efficiency over the existing single-phase two-stage approach. The necessary theory and computer simulations are developed to model and analyse the performance characteristics of the system. This thesis examines the new three-phase power converter topology and evaluates the performance of the design with respect to telecommunication industry expectations. Chapter 2 discusses the various single-phase topologies used and highlights the limitations of these designs. Chapter 3 continues with describing the various three-phase designs available and discusses the particular advantages and disadvantages of these systems. In chapter 4 the new topology is introduced, with simulations showing the theoretical performance, as well as the control strategies that are necessary. A new three-phase phase-locked loop is introduced and modelled in chapter 5, with results showing the performance characteristics which are discussed. Chapter 6 describes the details of the power converter topology and the implementation of the digital control processes necessary for the operation of the power converter. A detailed control model is derived for the system in chapter 7, and a stability analysis is performed. Chapter 8 details the results of various tests that are carried out on the power converter to determine the viability of the system as a potential commercial product. Finally, chapter 9 summarises the thesis, and points to areas of future research relating to further development of the power converter.

1.5 REFERENCES

[1] ITU-T Recommendation P800, "Methods for Subjective Determination of Transmission Quality", International Telecommunications Union, Telecommunication Standardisation Sector, 1996.

[2] Z.P. Fang, L. Chen and F. Zang, "Simple Topologies of PWM AC-AC Converters", IEEE Power Electronics Letters", Vol. 1, No. 1, pp. 10-13, March 2003.

[3] Electromagnetic Compatibility (EMC)-Part 3: Limits-Section 2: Limits for Harmonic Current Emissions, IEC 1000-3-2, 1st ed., 1995.

[4] M.A. Golkar, "Electrical Power Quality: Types and Measurements", IEEE International Conference on Electric Utility Deregulation, Restructuring and Power Technologies, Vol. 1, pp. 317-321, April 2004.

[5] P. Jain, J. Valerio and P. Jain, "A Review of Single Phase Power Factor Correction Circuits for Telecommunication Applications", International Telecommunications Energy Conference, pp. 334-338, Nov. 1994.

[6] D. James, "A Constant Power Rectifier for Telecommunications Using a Novel Variable Turns Ratio Transformer", International Telecommunications Energy Conference, pp. 251-256, Oct. 1997.

[7] O. Garcia, J. Cobos, R. Prieto, P. Alou and J. Uceda, "Single Phase Power Factor Correction: A Survey", IEEE Transactions On Power Electronics, Vol. 18, No. 3, pp. 749-755, May 2003.

[8] C. Ashton, "Ultra Capacitors for Short Duration Backup of DSL Cabinets", International Telecommunications Energy Conference, pp. 210-215, Sept. 2006.

[9] S. Li, S. Bassan and G. Moschopoulos, “Higher and Lower Power Single-Stage AC-DC Converters”, International Telecommunications Energy Conference, pp. 249-255, Sept. 2006.

[10] A. Pietkiewitz, D. Tollik, “Single-Stage Power Factor Corrected Rectifier Topology”, International Telecommunications Energy Conference, 6pp., June 1999.

[11] Z. Yang and P.C. Sen, “Recent Developments in High Power Factor Switch-mode Converters”, IEEE Canadian Conference on Electrical and Computer Engineering, Vol 2, pp 477-480, May 1998.

[12] I. Lindroth, P. Melchert and T. Sahlstrom, “Methods of Improving Efficiency in Wide Input Range Boost Converters at Low Input Voltages”, International Telecommunications Energy Conference, pp. 424-431, Sep. 2000.

[13] A.S. Kislovski, “Fast Active Inrush Current Limiter for Boost-Based Resistor Emulators”, International Telecommunications Energy Conference, pp. 649-652, Oct. 1994.

2 EXISTING SINGLE-PHASE TOPOLOGIES

In this chapter a study is conducted into the various single-phase topologies available that could be used in the telecommunications industry, and the reasons for the use of the single-phase two-stage approach being highlighted. Various other single-phase topologies are also investigated, and their suitability as telecommunication power converters is discussed.

The traditional two-stage power converter topology has been a popular choice for single-phase telecommunication power converter systems. This is due to the ability of the power converter system to provide both PFC and tight output voltage regulation, which guarantees compliance with the IEC1000-3-2 standard and the psophometric standard. The popularity of this topology can be attributed to the following reasons:

- Achieves sinusoidal line current.
- Provides good performance under universal line voltage.
- Presents many options for isolation.
- Has a constant 2^{nd} stage input voltage, which allows for optimal design of the second stage.

In general, telecommunication power converter systems consist of a non-isolated PFC stage, used to force the line current to follow the line voltage. This PFC stage creates an intermediate DC voltage with a relatively large second harmonic ripple, due to the single-phase nature of the power flow as well as its low bandwidth control [1]. The fact that there is a second harmonic ripple necessitates the use of a large storage capacitor (see Fig. 2.1). The second stage consists of a DC-

DC converter, providing isolation and high bandwidth output voltage regulation. This topology requires the use of two controllers, the first being a PFC controller, which consists of a current and voltage loop; and, the second, a DC-DC controller, which requires only a voltage feedback loop.

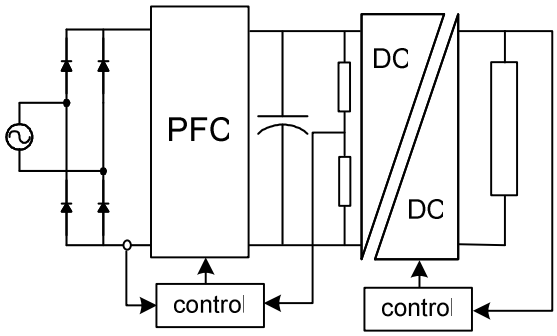


Fig. 2.1 Two-Stage Telecommunication Power Converter System

Considering the system from a power transfer point of view, the converter's input power oscillates at twice the mains frequency, and, in a single-phase system, because there can be no natural energy transfer from source to load at the mains zero crossing, an energy storage medium, normally in the form of a capacitor, is always required. In a single-phase system, the total DC power that can be delivered to the load is half the peak input power as illustrated in Fig. 2.2. The area under the DC power line of the positive half line cycle constitutes 68% of the input power, while the area above the DC power line consists of the remaining 32% of the input power. This 32% excess power is stored and then used later in each cycle, when the input power drops below the required output DC power.

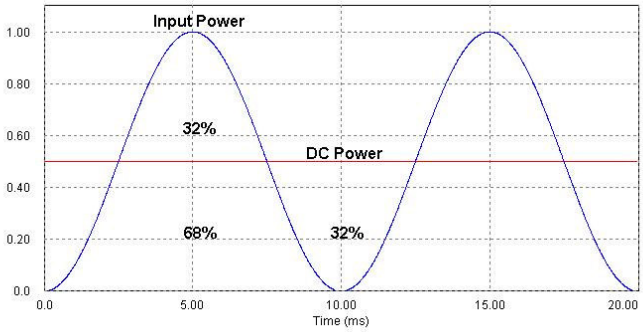


Fig. 2.2 Single-Phase Normalised Energy Transfer

Many authors have investigated methods of improving the traditional two-stage single-phase power converter system. These include using a voltage follower approach, where the power converter system is designed to work in a discontinuous conduction mode, making it a natural voltage follower, hence, the PFC current loop can be removed [2-5], resulting in a simplification of the control circuit. The use of passive filters is another method, whereby using reactive elements, it is possible to obtain near sinusoidal line current [6] without the use of a PFC stage. Other attempts have been undertaken to decrease the amount of energy processing in power converter systems compared with the two-stage approach, where the output power is processed twice [7-10]. In addition, there have also been attempts to improve the PFC stage in the conventional two-stage design. These include using multi-level topologies [11, 12] as well as the use of soft-switched [13] and resonant topologies [14-19], to reduce switching loss and thereby increase the power converter system efficiency. Several authors have introduced single-stage PFC converter topologies, which offer some advantages. However, their field of application is limited to low power [20-23]. All of the above mentioned techniques are discussed further in this chapter, in more detail, with the emphasis on the suitability and realisation effort of each topology, with regard to usage in the telecommunication power converter market.

2.1 Voltage Follower Power Converter Systems

A boost converter operating in continuous conduction mode, using the multiplier approach, is commonly used as a power factor correction topology due to its excellent performance [2]. Recently, power factor correction topologies derived from the buck-boost converter have been proposed, mainly because they emulate a natural resistor load when operating in the discontinuous conduction mode. It has been proposed by various authors that, using buck-boost derived topologies, which are natural voltage followers, the current control loop can be removed and, in so doing, provide a simpler control circuit [3-5]. In using these topologies, it would be possible to comply with the IEC1000-3-2 and the psophometric standards, with a second stage only needed if a non-isolated buck-boost derived topology was used. Therefore, it is possible to implement this approach as a single-stage solution. However, there is a disadvantage in the fact that these topologies are limited to low power applications only.

2.2 Power Converter System using Passive Filtering

Under the passive PFC approach, the use of LC input filters is required, providing a method that is both simple and reliable (Fig. 2.3). In using this technique, it becomes possible to draw close to sinusoidal current, thereby requiring only a DC-DC converter [6]. This means a single-stage power converter system can be implemented. The use of passive filtering also makes it possible to gain compliance with the IEC1000-3-2 standard. The DC-DC converter stage must provide isolation, voltage transformation and output voltage ripple reduction, thus achieving compliance with the psophometric standard. A disadvantage with using this approach is that the input filter tends to be bulky and heavy, which is due to the fact that the passive components are operating at line frequencies (50/60 Hz), resulting in the use of large reactive components.

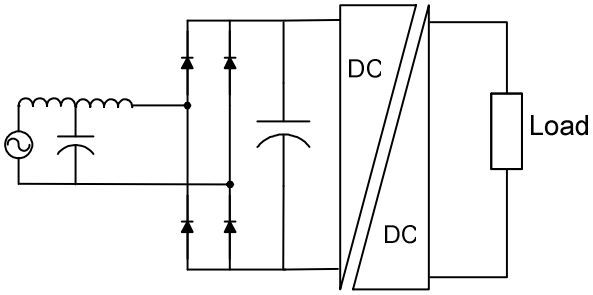


Fig. 2.3 Power Converter System using Passive Filtering

2.3 Power Converter Systems with Improved Energy Processing

2.3.1 Power Converter System with Shunt Regulator

A topology is proposed in [7] with the aim of the design to reduce the amount of power processing required and, in so doing, reducing the overall system losses (Fig. 2.4). The topology operates by having the PFC stage control the input current, and the DC-DC regulator stage controlling the output current, thus providing the regulation. The DC-DC regulator absorbs 32% of the average input power, which is the difference between the input and output power within a half line cycle (see Fig. 2.2), and then releases it to the load at the appropriate time, providing a constant flow of power to the load during the mains zero crossings. Since 68% of the average input power can reach the output through one power conversion stage, with only the remaining 32% needing to be processed twice, the average output power is therefore processed 1.64 times with this topology, instead of twice as with the traditional power converter. This topology does however require a large storage capacitor to hold up the output when the input is in a low portion of the line cycle. In using this type of topology, it would be possible to comply with the IEC1000-3-2 and the psophometric standard, however, this topology needs isolation on both the PFC and DC-DC regulator stage in order to meet with telecommunication industry requirements. Also, the DC-DC stage requires bi-directional power flow capability, which increases the overall design complexity.

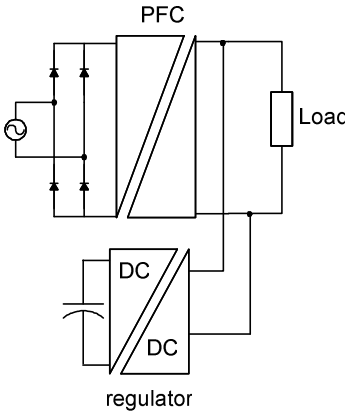


Fig. 2.4 Power Converter System with Shunt Regulator

2.3.2 Power Converter System with Harmonic Reducer

The topology proposed in [8] uses a bi-directional DC-DC converter to perform the function of the PFC stage as shown in Fig. 2.5. The bi-directional DC-DC converter takes the role of an active filter in reducing harmonic currents drawn from the mains. As a result, the power converter system would be able to comply with the IEC1000-3-2 standard. A DC-DC output stage is required for isolation, voltage transformation and ripple reduction. Accordingly, using this topology, it would be possible to comply with the necessary telecommunication standards. Also, similar to the Shunt Regulator topology discussed in section 2.3.1 the average output power is processed 1.64 times.

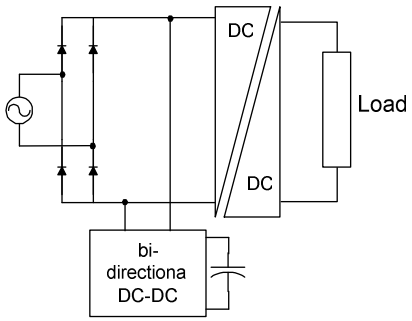


Fig. 2.5 Power Converter System with Harmonic Reducer

2.3.3 Power Converter System with Active Filtering

The topology shown in Fig. 2.6 is a variation of that discussed in section 2.3.2 in that the active filter is now placed on the mains side [9, 10]. The active filter is a four quadrant converter and is responsible for maintaining a sinusoidal line current, i.e. performing the PFC function. The DC-DC converter stage is used for isolation, voltage transformation and ripple reduction. Using this topology, it would be possible to comply with the required telecommunication standards. This topology also results in the average output power being processed 1.64 times, but has the disadvantage in that the active filter is a four quadrant converter requiring four switches, compared with the two quadrant bi-directional converter discussed in section 2.3.2, which requires only two switches.

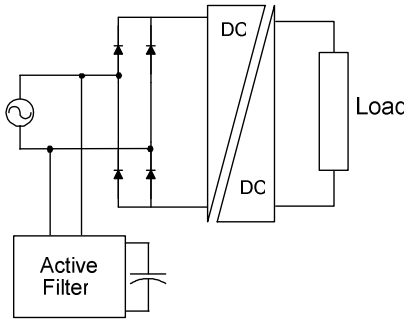


Fig. 2.6 Power Converter System with Active Filtering

2.4 Improved PFC Stage Designs

There have been many papers published about the overall efficiency of the conventional two-stage power converter system and how it can be improved by reducing the losses experienced in the PFC stage, which has traditionally used a hard-switched boost topology. These various methods are discussed in the following subsections.

2.4.1 Multi-Level Boost Converter

A method to reduce the switching losses in the boost converter stage is to use a multi-level topology and, in so doing, double the number of switching devices required (see Fig. 2.7). This results in reduced voltage stress, thus lowering the voltage rating requirements for the semiconductors [11]. An increase in efficiency over the conventional hard-switched boost topology was noted [12], but this is offset by the additional requirement of extra components.

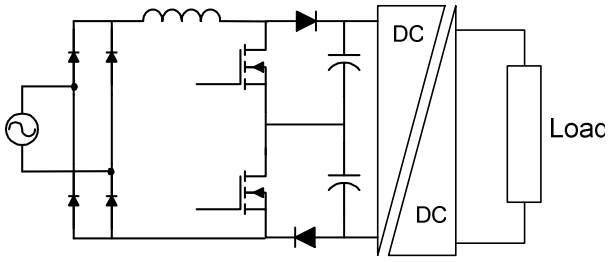


Fig. 2.7 Two-Stage Converter with Multi-Level Boost

2.4.2 Soft-Switched Boost Converter

The soft-switching boost converter approach combines PWM mode and resonant mode techniques. A topology is proposed in [13] that operates in PWM mode during most of the switching cycle, but operates in a resonant mode during the main boost switch turn-on and turn-off intervals (Fig. 2.8). As a result, zero voltage switching (ZVS) takes place in both the boost switch, as well as the output diode, and, in so doing, reduces the switching losses encountered by hard-switched boost converters. This solution requires an additional switch as well as some reactive elements. The authors reported a 2% increase in efficiency over a hard switched boost converter. However, this gain in efficiency is offset by the need for additional components and control circuitry. An alternative is to replace the diode bridge rectifiers and other diode components with switches,

thereby reducing the conduction losses [14]. This however does makes the soft switching strategy more complicated due to the addition of auxiliary circuits with active switches that are connected to the main power circuit. This can be made easier by using quasi-resonant techniques [15].

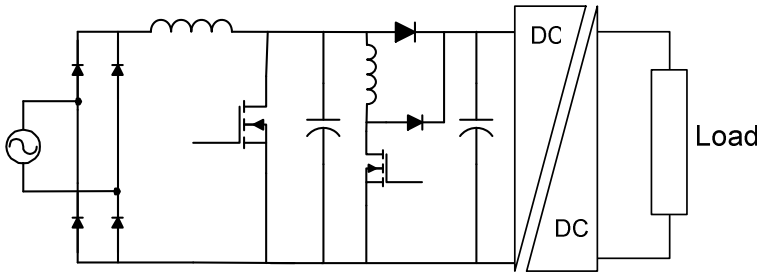


Fig. 2.8 Two-Stage Converter with Soft Switched Boost

2.4.3 Resonant PFC Designs

In a resonant power converter, voltage across a switch or current through a switch is shaped by the resonance of the inductive and capacitive elements. When the voltage or current becomes zero, the switch is then turned on or off, thus, reducing the switching loss. A PFC technique is proposed in [16] and [17] that uses a parallel and series resonant topology respectively. A high power factor is achieved by the natural boosting characteristic of the resonant topology. A major disadvantage is the high voltage and current stresses on the switches as well as the use of variable frequency control. Another approach is to place a resonant network between the input diode rectifier and the DC-DC converter [18, 19]. However, this results in a complex arrangement of reactive components for the resonant network, with no clear advantage over the traditional boost converter.

2.5 Single-Stage Power Converter

Many authors have attempted to find alternative solutions to the traditional two-stage power converter topology in order to reduce the cost and complexity associated with operating two separate power converters. The use of an active single-stage power converter requires only one controller and is, therefore, an advantage when compared to the two-stage approach. Also, being a single-stage, the output power is only processed once, giving it a theoretical efficiency advantage over a conventional two-stage approach. Many different power converter topologies have been proposed that integrate functions of PFC and isolated DC-DC conversion in a single stage [20-23], thus, maintaining telecommunication compliance requirements. However, a major problem with any single-stage approach is the fact that the voltage on the internal bulk capacitors varies with the line voltage and load current. This can result in high peak voltages, which makes these circuits impractical above about 200W due to the high cost of the storage capacitors required [24].

2.6 Summary

Due to the various requirements of the telecommunication industry, it is necessary to design telecommunication power converter systems to meet certain criteria. As a result, the common two-stage converter topology is used, with the first stage providing PFC, in order to comply with the IEC1000-3-2 standard, as well as the use of a DC-DC converter to comply with the psophometric standard. There have been many attempts to improve on the two-stage design while still meeting the industry requirements. Among them are the single-stage topologies that provide an increased efficiency over the two-stage converter, but are limited to low power applications only. The passive PFC converter is a single-stage design, with only a DC-DC converter required. The use of passive input filters provides sinusoidal input current shaping. These passive filters use large bulk reactive components which increase the cost and make this design solution not commercially viable in the medium to high power range. In using the voltage follower concept, it allows for a simple PFC controller. However, due to the topologies used by the authors, this type of converter is also restricted to low power applications. A method of increasing the overall efficiency of the power converter system is to rearrange the power processing blocks to reduce the amount of power that is handled. Although it has been shown to result in an increase in the efficiency over the two-stage converter, more complex control and switching devices are required. Other methods discussed, regarding optimisation of the traditional two-stage converter by using multi-level and resonant topologies, can result in increased efficiency. However, this also comes with the cost of extra componentry. There is therefore no significant decrease in the dollar per watt ratio, in using these alternative designs, when compared to the conventional two-stage power converter topology. Table 1 lists the comparisons of various features of the mentioned topologies.

	Traditional 2 stage	Isolated Buck-Boost	Passive Input Filtering	Shunt Regulator	Harmonic Reducer	Active Filtering	Multi-Level Boost	Soft Switched Boost	Resonant PFC	Single-Stage
PFC	0.99	0.99	0.9	0.99	0.99	0.99	0.99	0.99	0.99	0.99
current THD %	<5	>5	>5	>5	<5	<5	<5	<5	<5	>5
control	complex	simple	simple	complex	complex	complex	complex	complex	complex	complex
power (kW)	<6	<0.2	<1	<6	<6	<6	<6	<6	<0.2	<0.2
efficiency %	90	95	95	90	90	90	92	92	95	90
chokes	2	1	1	2	2	2	2	2	1	1
switches	5	1	4	4	6	8	6	6	4	1
comments		poor utilization factor	bulky input filtering	isolated boost required	2 quadrant	4 quadrant	extra components	extra components	HV stresses	HV stresses

Table 1 Comparison of Performance Factors of Single-Phase Telecommunication Topologies

2.7 Conclusion

It is possible to increase the efficiency of a power converter system using designs other than the traditional two-stage converter topology, however, this does come at the expense of additional control circuitry, switching devices and, or, reactive elements. Accordingly, there is no definite cost advantage in using these designs over the traditional two-stage power converter system. The limitations encountered by single-phase power converter systems are due to the fact that a single-phase supply does not provide a constant power source, but a time varying one and, hence, energy storage is always required.

In order to realise a power converter system where energy storage is no longer needed, it becomes necessary to look at possibilities in a three-phase system which presents an ideal constant power source. In the next chapter, three-phase power converter topologies are explored and discussed.

2.8 REFERENCES

[1] B. Sharifipour, J.S. Huang, P. Liao, L. Huber and M.M. Jovanovic, "Manufacturing and Cost Analysis of Power Factor Correction Circuits", IEEE Applied Power Electronics Conference and Exposition, Vol. 1, pp. 490-494, Feb. 1998.

[2] M. Hernandez, C. Aguilar, J. Arau, J. Sebastian and J. Uceda, "Comparative Analysis of Boost and Buck-Boost Derived topologies Used as Power Factor Correctors", IEEE Power Electronics Conference, pp. 14-19, Oct. 1995.

[3] R. Erickson, M. Madigan and S. Singer, “Design of a Simple High-Power-Factor Rectifier Based on the Flyback Converter”, IEEE Applied Power Electronics Conference and Exposition, pp. 792-801, March 1990.

[4] M. Brkovic and S. Cuk, “Input Current Shaper using Cuk Converter”, IEEE International Telecommunications Energy Conference, pp.532-539, Oct. 1992.

[5] J. Sebastian, J. Uceda and F.S. Reis , “Power Factor Preregulators employing the Flyback and Zeta Converters in FM Mode”, IEEE Power Electronics Congress, pp. 132-137, Oct. 1996.

[6] W.M. Lin, M.M. Hernando, A. Fernandez, J. Sebastian and P.J. Villegas, “A New Topology for Passive Circuit Design to Allow AC-to-DC Converters to Comply with the New Version of IEC 1000-3-2 Regulations”, IEEE Power Electronics Specialists Conference, Vol. 4, pp. 2050-2055, June 2002.

[7] J. Gegner, C. Hung and C. Lee, “High Power Factor AC-to-DC Converter Using a Reactive Shunt Regulator”, IEEE Power Electronics Specialists Conference, Vol. 1, pp. 349-355, June 1994.

[8] O. Garcia, M. Avial, J. Cobos, J. Uceda, J. Gonzales and J. Navas, “Harmonic Reducer Converter”, IEEE Transactions on Industrial Electronics, Vol. 50, No. 2, pp. 322-327, April 2003.

[9] B.R. Lin and D.J. Chen, “Single-phase neutral point clamped AC/DC Converter with the Function of Power Factor Corrector and Active Filter”, IEE Proceedings of Electric Power Applications, Vol. 149, pp. 19-30, Jan. 2002.

[10] Z.F. Hussien, N. Atan and I.Z. Abidin, “Shunt Active Power Filter for Harmonic Compensation of Nonlinear Loads”, International Power Engineering Conference, pp. 117-120, Dec. 2003.

[11] M.T. Zang, Y. Jiang, F.C. Lee and M. Jovanovic, "Single-Phase Three-Level Boost Power Factor Correction Converter", Applied Power Electronics Conference and Exposition, Vol. 1, 435-439, March 1995.

[12] B. Lin and S. Hung, "A Single Phase Three-Level Boost Type Rectifier", International Symposium on Circuits and Systems, Vol. 4, pp. 353-356, May 2002.

[13] G. Hau, C.S. Leu and F.C. Lee, "Novel Zero Voltage Transition PWM Converters", IEEE Transactions on Power Electronics, Vol. 9, pp. 213-219, March 1994.

[14] A. Jangwanitlert and J. Songboonkaew, "A Soft-Switched AC-DC Symmetrical Boost Converter with Power Factor Correction", Power Electronics and Drive Systems Conference, pp.784-788, November 2007.

[15] I. Barbi and S.A. Oliveira da Silva, "Sinusoidal Line Current Rectification at Unity Power Factor with Boost Quasi-Resonant Converters", Applied Power Electronics Conference and Exposition, pp. 553-562, March 1990.

[16] M.J. Shutten, R.L. Steigerwald and M.H. Kherulawala, "Characteristics of Load Resonant Converters Operated in a High-Power Factor Mode", IEEE Transactions on Power Electronics, Vol. 7, No. 2, pp. 304-314, April 1992.

[17] W. Sulistyono and P.N. Enjeti, "A Series Resonant AC-to-DC Rectifier with High-Frequency Isolation", IEEE Transactions on Power Electronics, Vol. 10, No. 6, pp. 784-790, Nov. 1995.

[18] M.H. Kherulawala, R.L. Steigerwald and R. Gurumoorthy, "A Fast-Response High Power Factor Converter with a Single Power Stage", IEEE Power Electronics Specialists Conference, pp. 769-779, June 1991.

[19] J. Qian and F.Lee, “A High Efficient Single Stage Single Switch High Power Factor AC/DC Converter with Universal Input”, IEEE Applied Power Electronics Conference and Exposition, Vol. 1, pp. 281-287, Feb. 1997.

[20] L. Huber and M.M. Jovanovic, “Single Stage Single Switch Isolated Power Supply Technique with Input Current Shaping and Fast Output Voltage Regulation for Universal Input Voltage Range Applications”, IEEE Applied Electronics Conference, Vol. 1, pp. 272-280, Feb. 1997.

[21] J. Sebasian, M.M. Hernando, P. Villegas, J. Diaz and A. Fontan, “Input Current Shaper based on the Series Connection of a Voltage Source and a Loss Free Resistor”, IEEE Applied Electronics Conference, Vol. 37, No. 2, pp. 583-591, March 2001.

[22] O. Garcia, J.A. Cobus, R. Prieto, P. Alou and J. Uceda, “Simple AC/DC Converters to Meet IEC1000-3-2”, IEEE Applied Power Electronics Conference and Exposition, Vol. 1, pp. 487-493, Feb. 2000.

[23] O. Garcia, J.A. Cobus, R. Prieto, P. Alou and J. Uceda, “Design Trade-Offs of Bi-Flyback and Bi-Forward AC/DC Converters to Comply Low Frequency Harmonic Regulation”, IEEE Power Electronics Specialist Conference, Vol. 2, pp. 999-1004, June 2000.

[24] C. Qiao and K.M. Smedley, “A Topology Survey of Single-Stage Power Factor Corrector with a Boost Type Input-Current-Shaper”, IEEE Transactions on Power Electronics, Vol. 16, No. 3,

pp. 360-368, May 2001.

3 EXISTING THREE-PHASE TOPOLOGIES

A three-phase system has certain inherent advantages over a single-phase system, with the most obvious being the constant flow of power available; hence, energy storage is no longer required. A three-phase system, from a pragmatic point of view, offers more supply integrity over a single-phase system. A single-phase system requires additional phase-neutral protection and is more susceptible to imbalances and harmonics. Also, the availability of a neutral is known to be an issue in many installations.

This chapter discusses the nature of three-phase power and reports the different types of three-phase topologies that could be used as telecommunication power converters. The topologies are discussed and various strengths and weakness highlighted.

In an ideal three-phase system, there is a continuous energy transfer from source to load, and the total power transferred is the sum of the power from the three individual phases. In a three-phase system with resistive phase loads, the power drawn by each phase is given by the following formula:

$P = \frac{V_p{}^2 \sin^2 \theta}{R}$ where V_p= peak input voltage and θ = phase angle

Assuming that the voltage is unchanging

$\frac{V_p{}^2}{R} = k$ where k is a constant

$\therefore P = k \sin^2 \theta$

The total power transfer P_{total} for a three-phase system assuming that the voltage is unchanging and R is fixed is given as

$$P_{total} = k\sin^2\theta + k\sin^2(\theta + 120^o) + k\sin^2(\theta + 240^o)$$

$$= \frac{k}{2}[3 - \cos 2\theta - \cos(2\theta + 240^o) - \cos(2\theta + 480^o)]$$

$$= \frac{k}{2}[3 - \cos 2\theta + \frac{1}{2}\cos 2\theta - \frac{\sqrt{3}}{2}\sin 2\theta + \frac{1}{2}\cos 2\theta + \frac{\sqrt{3}}{2}\sin 2\theta]$$

$$= \frac{3}{2}k$$

It can be seen that the power drawn per phase by a three-phase system has a $\sin^2\theta$ wave profile with the power in each phase summing together resulting in the total power being constant and equal to 1½ times the peak input power per phase as illustrated in Fig. 3.1.

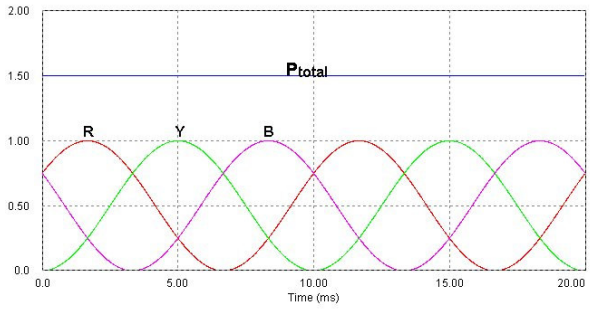


Fig. 3.1 Three-Phase Energy Transfer Model

A number of common three-phase topologies exist that could be realised as telecommunication power converter systems. Among those are the power converters that use passive input filtering in order to comply with the IEC1000-3-2 standard [1], however these do have size and weight issues making them not a very popular choice. Boost derived topologies are traditionally the topology of choice due to good current symmetry with numerous designs proposed by various authors [2-6]. A disadvantage with a boost derived topology is that unless bi-directional power flow is possible the circuit suffers from inrush currents during startup conditions. Several buck derived topologies

have been proposed [7-12] which offer some attractive features compared to the boost topology, such as inherent short circuit protection, easy inrush current control, and low output voltage. The use of modular topologies is gaining in popularity as they offer a natural redundancy and independent control of modules can ensure power supply continuity during non-ideal mains conditions [13-14]. The buck boost topology is another choice where inrush current control can be achieved, however this topology has efficiency penalties due to having at least two power semiconductors in the input current path as well as having a poor silicon utilisation factor [15-19]. These mentioned topologies are discussed in more detail further in the chapter with the emphasis on the suitability and realisation effort of each topology, with regard to usage in the telecommunication power converter market.

3.1 Power Converter Topology using Passive Input Filters

A technique that uses passive input filters is described in [1], the aim being to reduce the large 5^{th} and 7^{th} harmonic current components, this is shown in Fig. 3.2. The passive elements decrease the total harmonic distortion by filtering out the low frequency harmonics, thus, improving the current waveforms drawn from the supply. The storage capacitor is not required for energy storage, but for ripple reduction and, hence, has a reduced size compared with the single-phase passive approach. This technique has several disadvantages; one being the size and weight requirements of the filter elements; the second, being the difficulty in tuning the filter if the AC line and source impedances are unknown; and the third, is the difficulty in designing the appropriate components so that the desired PFC occurs for wide variations in input AC voltage. In using this approach, it is possible to comply with the IEC1000-3-2 standard. However, a DC-DC converter stage is still needed to provide isolation, voltage transformation and ripple reduction and, hence, compliance with the psophometric standard.

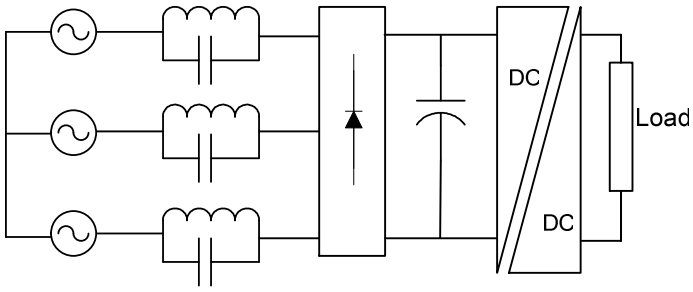


Fig. 3.2 Power Converter with Passive Input Filters

3.2 Boost Derived Power Converter Topologies

Three-phase boost PFC power converters have traditionally been the preferred topology for high power applications due to their symmetric current drawing characteristics. A disadvantage to any boost derived topology is the inability to control startup inrush currents and output short circuit conditions, unless bi-directional power flow is possible. The following subsections describe various boost derived topologies.

3.2.1 Six Switch Boost Power Converter

A common six switch boost converter topology has the ability to operate as a rectifier as well as an inverter due to the bidirectional power flowing capabilities (Fig. 3.3). It also has good current quality and low EMI emissions [2]. The use of bidirectional switches also results in the ability to control the output voltage down to zero, thus, eliminating the problem that boost topologies have with regard to startup inrush currents and output short circuit protection. Unidirectional switches can be used for simplicity at the expense of current control capabilities. The converter is controlled by an output voltage loop for output regulation, and inner current loops which shape the input currents according to their sinusoidal references. The input inductors form part of the boost topology and, as such, work at the switching frequency. As a result, input inductors operating at

switching frequencies are smaller in size compared with line frequency input inductors. Both the IEC1000-3-2 standard and the psophometric standard can be met with this topology, thus, the DC-DC stage is only needed for isolation and voltage transformation.

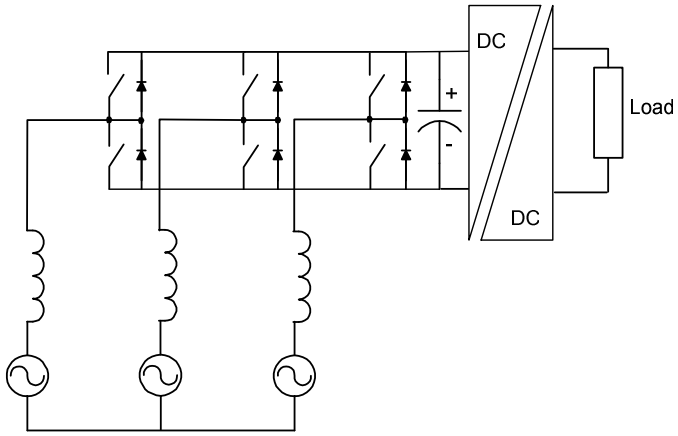


Fig. 3.3 Six Switch Boost Power Converter System

3.2.2 Four Switch Boost Power Converter

The boost derived converter shown in Fig. 3.4, and proposed in [3], has three boost inductors in the AC lines, four active switches and two series connected capacitors. The boost derived converter is capable of bi-directional power flow and, thus, is able to control the output voltage down to zero. The converter performs PFC by taking advantage of the fact that if two of the three line currents in a balanced three-phase system are controlled, the third is automatically constrained. This removes the need for a third converter leg. A disadvantage is that even with a slight imbalance in the supply system, the converter performance may deteriorate considerably. In using this approach, it is possible to comply with the IEC1000-3-2 standard. However, a DC-DC converter stage is still needed to provide isolation, voltage transformation and ripple reduction.

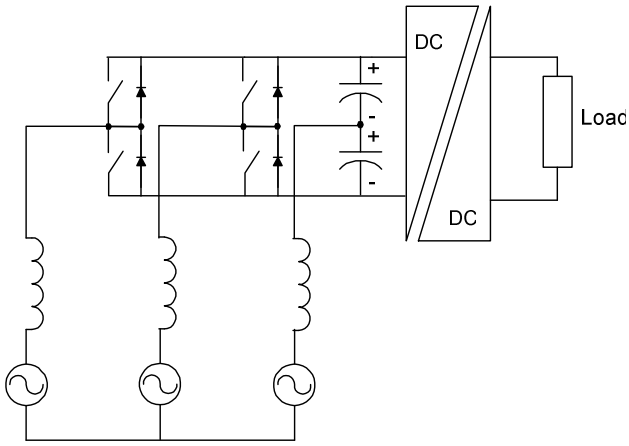


Fig. 3.4 Four Switch Boost Power Converter System

3.2.3 Three Switch Boost Power Converter

The three switch boost derived converter proposed in [4] works on the principle of current control. When two switches are conducting, the phase with the larger supply voltage is connected to the positive rail, while the phase with the smaller supply voltage is connected to the negative rail (Fig. 3.5). As a result, the phase shift angle between the modulation references and supply voltages can be at most 30^{o}. Accordingly, this topology cannot be used for bi-directional power flow. As a result, this topology suffers from startup inrush currents and, also, uncontrolled negative half cycles on all phases and fluctuations in the DC bus voltage. In using this topology, it is possible to comply with the IEC1000-3-2 standard. However, a DC-DC converter stage is still needed to provide isolation, voltage transformation and ripple reduction.

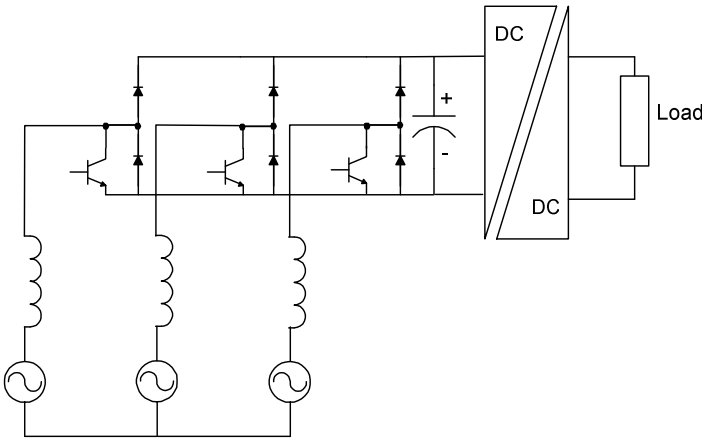


Fig. 3.5 Three Switch Boost Power Converter System

3.2.4 Vienna Rectifier

Another three-switch boost derived converter, also called the Vienna rectifier, is a unidirectional three-level PWM converter (Fig. 3.6) and, as a result, suffers from startup inrush currents. The input stage creates a DC voltage across the two switches connected to the transformer primary. These two switches, in turn, regulate the voltage being applied to the primary of the transformer. Accordingly, they are able to control the output voltage generated [5]. The Vienna rectifier has a complex control system and requires special semiconductor module fabrication. It is possible to comply with the telecommunication standards using this topology with no additional second stage needed.

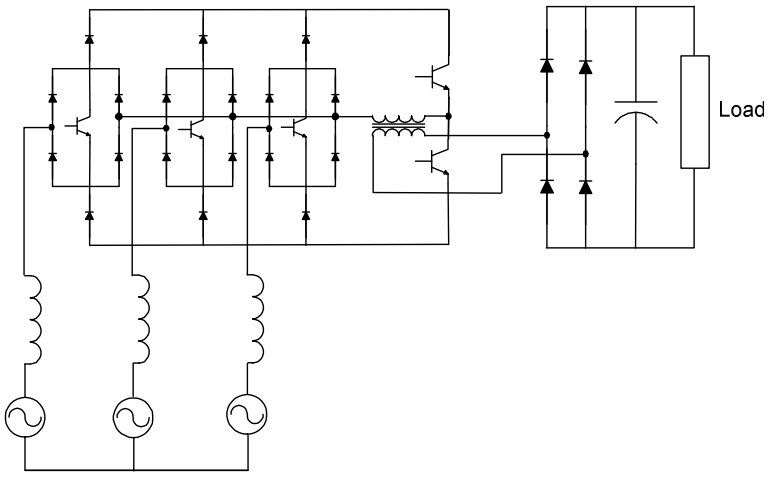


Fig. 3.6 Vienna Rectifier

3.2.5 Single Switch Boost Power Converter

The single switch boost converter topology proposed in [6] has an LC type input filter and, with the boost switch turned on at a constant frequency, the duty cycle is controlled such that the input current is always discontinuous (Fig. 3.7). During the on-period of the boost switch, all three input phases become shorted through the input inductors, the six rectifier diodes and the boost switch. The three input currents begin simultaneously to increase at a rate proportional to the instantaneous values of their respective phase voltages. The specific peak current values during each on-interval are proportional to the average values of their input phase voltages during the same on-interval. The result is that each AC line current is a discontinuous waveform made up of a train of triangular pulses bounded by a sinusoidal envelope. In using this topology it is possible to comply with the IEC1000-3-2 standard. However, a DC-DC converter is needed for isolation, voltage transformation and ripple reduction.

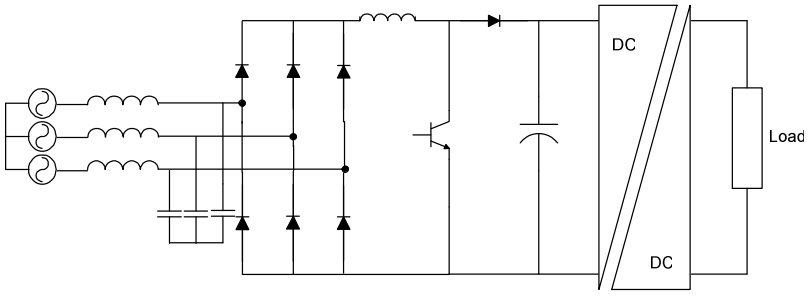


Fig. 3.7 Single Switch Boost Power Converter

3.3 Buck Derived Power Converter Topologies

A buck derived topology has some attractive features compared to the boost topology, such as inherent short circuit protection, easy inrush current control, and low output voltage. In addition, its input currents can be controlled in open loop, and much wider voltage loop bandwidth can be achieved [7]. Several three-phase buck derived topologies are discussed in the following subsections.

3.3.1 Six Switch Single-Stage Buck Power Converter

A basic six-switch isolated buck converter is shown in Fig. 3.8. This type of converter directly converts the three-phase AC to DC in a single isolated buck-derived stage by splitting the conversion process into a three-phase cyclo-converter section. This is then used to synthesise the high frequency AC voltage from the three-phase input voltages. The secondary AC signal is rectified and filtered to obtain the desired output DC voltage. The switching sequence of this type of converter can be implemented by either a look-up table or by an analogue derived PWM circuit with distribution logic. This type of converter can be implemented as a hard switched [8] or soft switched type [9]. This topology can meet with all the telecommunication standards. However, it has the disadvantage of requiring AC switches and a complex control system.

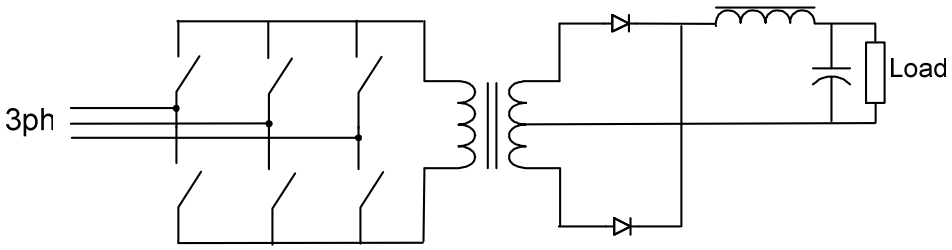


Fig. 3.8 Six Switch Single-Stage Buck Converter

3.3.2 Six Switch Two-Stage Buck Power Converter

A six switch buck derived converter proposed in [10] consists of IGBT switching devices connected in series with an ultra fast recovery diode, resulting in reverse voltage blocking capability and unidirectional current flow (see Fig. 3.9). The converter works on the principle of current control, and uses a direct phase control scheme based on a modulated space vector PWM method. This topology is able to meet all the telecommunication standards with a second stage needed only for isolation and voltage transformation. There is also a three switch version of the mentioned topology discussed in [11].

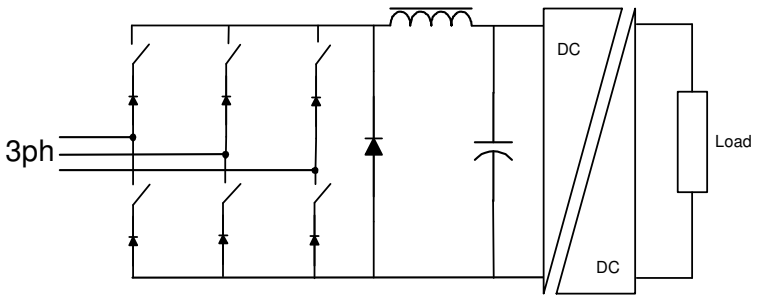


Fig. 3.9 Six Switch Two-Stage Buck Converter

3.3.3 Single Switch Buck Power Converter

The single switch buck converter, as seen in Fig. 3.10, operates by having the voltages across the input capacitors discontinuous [12], resulting in high voltage peaks across the switch. An improved topology is introduced in [13], which reduces the voltage stress across the switch. Using both topologies, it is possible to comply with the IEC1000-3-2 standard. However, a DC-DC converter is needed for isolation, voltage transformation and ripple reduction.

Both the single switch boost and buck topologies are limited in power because of the high stresses the switches must take. This is especially true of the buck converter, if the output voltage is low (i.e. 48V). In this case, the switch must remain open for a long time during the switching cycle. Accordingly, this results in the continual charging of the input capacitors, leading to high peak voltages across the switch.

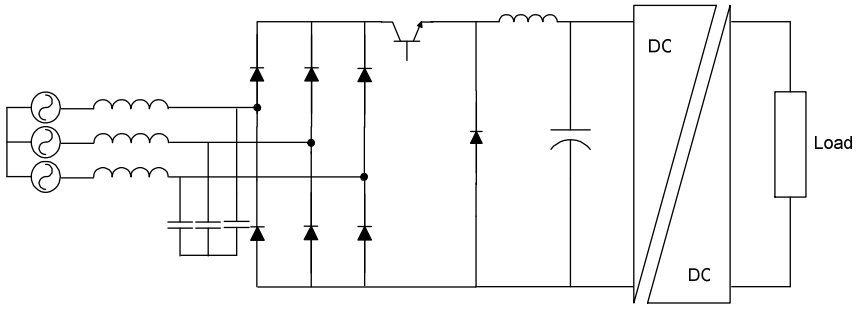


Fig. 3.10 Single Switch Buck Converter System

3.4 Modular Topologies

Three-phase AC-DC conversion can be realised by using three single-phase converter modules as shown in Fig. 3.11. Each converter module is a two-stage topology consisting of a PFC stage and a DC-DC stage providing connection to a common bus. The circuit has the advantage that it is a

well-known configuration and, therefore, easy to implement, as well as the fact that each converter module only carries ⅓ of the output power. The design is a three-phase solution using single-phase entities. It has the advantage that it can be realised in modular form, and provides a certain amount of redundancy as the three converters operate independently [14]. As a result of using standard single-phase topologies, all the telecommunication standards can be met. There is also a delta connected version of three single-phase modules described in [15].

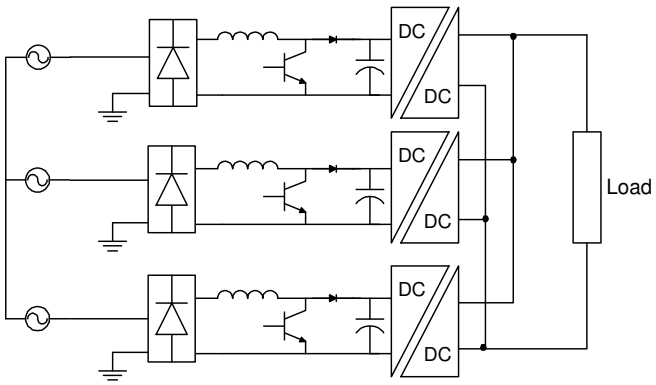


Fig. 3.11 Three Single-Phase Modules

A simplification to the topology described by Fig. 3.11 is shown in Fig. 3.12 where the outputs of the three boost converters are connected in parallel to a common DC-DC converter [16]. This method results in the PFC modules only transferring ⅓ of the output power, while the common DC-DC converter carries the full output power. Using this topology, it is also possible to comply with the necessary telecommunication standards.

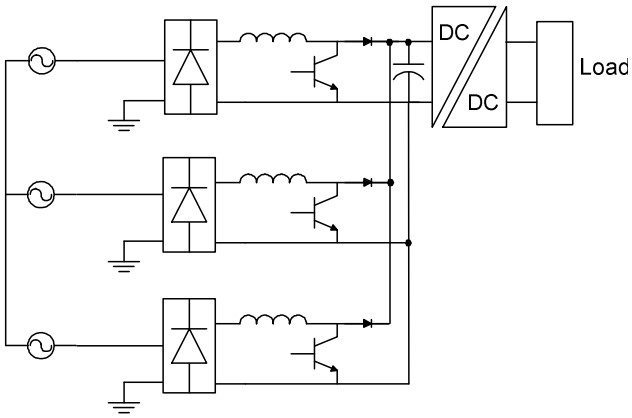


Fig. 3.12 Single-Phase Boost Modules with Common DC-DC Converter

3.5 Buck Boost Converter

The buck boost type converter has step-up and step-down output voltage characteristics, and also the capability of limiting the inrush and DC short circuit currents [17-20]. The existing three-phase buck topologies show some efficiency disadvantages, since they have at least two power semiconductors in the input current path [21]. This topology yields poor silicon utilisation due to a wide input-output voltage operating range. Also, since it is a non-isolating topology, isolation is required in order to comply with telecommunication standards.

3.6 Summary

There are various three-phase designs that could be used as telecommunication power converters. Many topologies require the addition of a second isolating DC-DC stage, which is necessary due to telecommunication industry requirements. These require a greater realisation effort, compared with the single-stage designs. They not only require additional components and magnetics, but also, additional control implementation. Boost derived topologies have the disadvantage of startup inrush currents; unless bi-directional power flow is possible, which requires AC switches and a complex control implementation. The passive PFC approach, although a single-stage, is impractical due to the size and weight of filtering components. The six switch single-stage buck derived topology offers possibilities over the single switch counterpart, which suffers high voltage stress and therefore has a limited power rating. It does, however, require bi-directional switches and a complicated PWM control strategy. The use of modular topologies is an attractive option, offering redundancy and the use of well known topologies which make for a simple design implementation. The buck boost converter has the ability to limit inrush currents, but exhibits poor silicon utilisation, rendering it as an ineffective cost solution. Table 1 compares various features of the mentioned topologies.

	Passive Input Filtering	6 Switch Boost	4 Switch Boost	3 Switch Boost	1 Switch Boost	Vienna	6 Switch Buck	6 Switch 2 stage Buck	1 Switch Buck	Modular	Buck Boost
PFC	0.9	0.99	0.99	0.99	0.99	0.99	0.99	0.99	0.99	0.99	0.99
current THD %	>5	<5	<5	>5	<5	<5	<5	<5	>5	>5	>5
control	simple	complex	simple	simple	simple	complex	complex	complex	simple	complex	complex
power (kW)	<10	<10	<5	<5	<6	<10	<10	<10	<6	<10	<6
efficiency %	95	90	90	92	92	93	92	92	90	90	85
chokes	4	4	4	4	2	3	1	2	2	4-6	2
switches	4	10	8	7	6	5	6	10	5	5	8
comments	bulky input filtering		Susceptible to Phase Imbalances	DC Bus Fluctuations		Isolated Topology	AC Switches	IGBT's	HV stresses	Inherent Redundancy	HV stresses

Table 1 Comparison of Performance Factors of Three-Phase Telecommunication Topologies

3.7 Conclusion

A converter topology is required that can meet all the necessary telecommunication industry standards. Also, in order to get the highest possible efficiency, the topology needs to be a single-stage design, as well as being a buck derived topology, to eliminate inrush current issues associated with boost derived topologies. The design should, ideally, be able to offer a certain amount of redundancy, thereby ensuring continued supply during module failure or mains anomalies. The system should, also, only require a single controller unit. A new converter topology that can meet all these requirements is introduced and discussed in the following chapter.

3.8 REFERENCES

[1] A. Prasad, P. Ziogas and S. Minias, " Passive Input Current Wave Shaping Method for Three-Phase Diode Rectifiers", Applied Power Electronics Conference and Exposition, pp. 319-330, March 1991.

[2] H. Mao, D. Boroyevich, A. Ravindra and F. Lee, "Analysis and Design of High Frequency Three-Phase Boost Rectifiers", Applied Power Electronics Conference and Exposition, Vol. 2 pp. 538-544, March 1996.

[3] B. Lin and D. Wu, "Implementation of Three-Phase Power Factor Correction Circuit with Less Power Switches and Current Sensors", IEEE Transactions on Aerospace and Electronic Systems, Vol. 34, pp. 664-670, April 1998.

[4] B. Singh, P. Jain and G. Joos, "Three-Phase PWM Voltage Source Rectifier with a Reduced Number of Switches", Canadian Conference on Electrical and Computer Engineering, Vol. 2, pp. 951-955, March 2000.

[5] J.W. Kolar, U. Drofenik, and F. Zach, "Vienna Rectifier II-A Novel Single-Stage High Frequency Isolated Three-Phase PWM Rectifier System", IEEE Transactions On Industrial Electronics, Vol. 46, No. 4, pp. 674-691, Aug. 1999.

[6] S. Ando, A Ueda and A. Torii, "Characteristics of Three-Phase Boost Type Rectifier with LC Filter in AC Side", Power Conversion Conference, Vol. 3, pp. 1211-1216, April 2002.

[7] H. Mao, F. Lee, D. Boroyevich and S. Hiti, "Review of High-Performance Three-Phase Power-Factor Correction Circuits", IEEE Transactions on Industrial Electronics, Vol. 44, No. 4, pp. 437-446, Aug. 1997.

[8] S. Manias, P. D. Ziogas, "A Novel Sinewave In AC to DC Converter with High Frequency Transformer Isolation", IEEE Transactions on Industrial Electronics, Vol. IE-32, No. 4, pp. 430-438, Nov. 1985.

[9] D. Borojevic, V. Vlatkovic, and F.C. Lee, "A Zero-Voltage Switched Three Phase PWM Switching Rectifier with Power Factor Correction", Power Electronics Specialists Conference, Vol. 2, pp. 1352-1360, June 1992.

[10] L. Yabin, L. Heming and Y. Peng, "A Unity Power Factor Three-Phase Buck Type SVPWM Rectifier Based on Direct Phase Control Scheme", IEEE Power Electronics and Motion Control Conference, Vol. 1, pp. 1-5, Aug. 2006.

[11] B.W. Williams, M Mirkazemi, D. Tooth and S.J. Finney, "A Three-Phase AC to DC Converter with Controllable Displacement Factor", Power Electronics Specialists Conference, Vol. 2, pp. 996-1000, June 1995.

[12] E. Ismail and R. Erickson, "Single-Switch 3Ø PWM Low Harmonic Rectifiers", IEEE Transactions on Power Electronics", Vol. 11, pp. 338-346, March 1996.

[13] J. Shah and G. Moschopoulos, "Three-Phase Rectifiers With Power Factor Correction", Canadian Conference on Electrical and Computer Engineering, pp. 2070-2073, May 2005.

[14] D. Chapman, D. James and D.A. Torrey, "A High Density 48V 200A Rectifier with Power Factor Correction – An Engineering Overview", International Telecommunications Energy Conference, Vol. 1, pp. 118-125, Sep. 1993.

[15] R. Greul, S.D. Round, J.W. Kolar, "The Delta Rectifier-Analysis, Control and Operation", IEEE Transactions on Power Electronics, vol. 21, no. 6, pp. 1637-1648, Nov. 2006.

[16] G. Spiazzi and F. C. Lee, "Implementation of Single-Phase Boost Power-Factor Correction Circuits in Three-Phase Applications", IEEE Transactions on Industrial Electronics, Vol. 44, pp. 365-371, June 1997.

[17] R. Itoh and K. Ishikaza, "Three-Phase Flyback AC-DC Converter with Sinusoidal Supply Currents", IEE Conference on Electric Power Applications, Vol. 138, No. 3, pp. 143-151, May 1991.

[18] C.T. Pan and T.C. Chen, "Step-Up/Down Three-Phase AC to DC Converter with Sinusoidal Input Current and Unity Power Factor", IEE Conference on Electric Power Applications, Vol. 141, No. 2, pp. 77-84, March 1994.

[19] Y. Nishida, A. Maeda and H. Tornita, "A New Instantaneous-Current Controller for Three-Phase Current Buck-Boost and Buck Converters with PFC Operation", Applied Power Electronics Conference and Exposition, APEC, pp. 875-883, March 1995.

[20] V.F. Pires and J.F. Silva, "Single-Stage Three-Phase Buck-Boost Type AC-DC Converter with High Power Factor", IEEE Transactions on Power Electronics, Vol. 16, No. 6, pp. 784-793, Nov. 2001.

[21] V.F. Pires and J.F. Silva, "Three-Phase Single-Stage Four-Switch PFC Buck-Boost-Type Rectifier", IEEE Transactions on Industrial Electronics, Vol. 52, No. 2, pp. 444-453, April 2005.

4 NEW TOPOLOGY CONCEPTS

A new three-phase topology is proposed that capitalises on the ability of a three-phase source to deliver constant power. The proposed topology uses three single-stage converters, with each converter connected across a single phase and controlled to perform a squaring function on the input voltage. Accordingly, this results in a second harmonic voltage waveform, which has the same profile as the natural power transferred to a resistive load. The power converter prototype takes the form of a ZVS full bridge converter with a current doubler output topology as seen in Fig. 4.1.

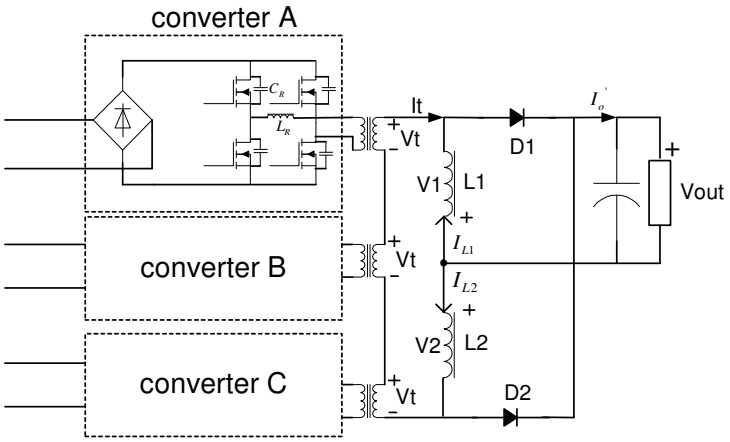


Fig. 4.1 Proposed Topology

The concept can be modelled by considering each converter as an ideal transformer performing a 1:V_{in} transfer function on the input voltage (see Fig. 4.2). Consequently, the secondary voltages have a power waveform profile, which sums to a constant due to the series connection of the transformer secondaries. If the load is considered resistive, the output current is also constant and unity power factor results. V_{in} varies over the range 0 to V_p ,with V_p the peak input voltage, and accordingly, this converter can be best realised by using a buck-derived topology.

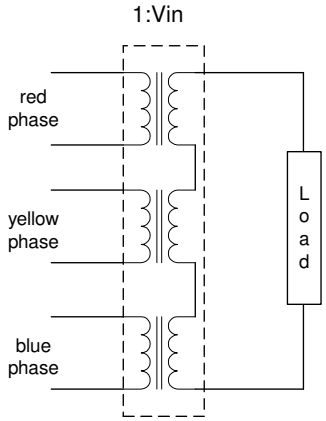


Fig. 4.2 Series Buck Converter

Ideally, the new converter system will have the following characteristics:

- Unity input power factor
- Zero output voltage ripple
- Single-stage converter
- Isolation
- Voltage transformation

The new converter system is to be an isolated topology, necessary for compliance with telecommunication functional and safety requirements. This topology offers high modularity and provides mains balancing, giving the possibility to deliver full output power in case of mains voltage imbalances, whilst using only a single controller. A unity power factor will satisfy the IEC1000-3-2 standard, and with theoretical zero output voltage ripple, compliance with the

psophometric standard is guaranteed. A single-stage design is an approach that is also expected to result in a more energy efficient power converter system.

4.1 Concept Simulations

As a preliminary investigation the series buck converter system was simulated using a package called PSIM 6. This system model is shown in Fig. 4.3 with the circuit consisting of a balanced three-phase 50Hz input voltage with unity magnitude. Three control blocks, each perform a V_{in}^2 transfer function on the input voltage with the outputs connected in series to a resistive load.

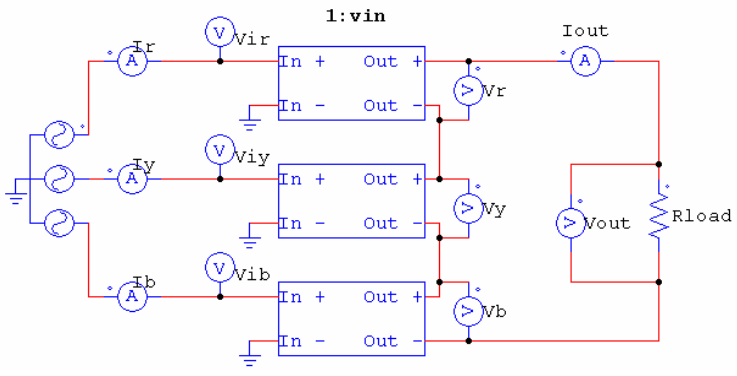


Fig. 4.3 Series Buck Topology

Fig. 4.4 shows the details of the control blocks used in the simulation. The multipliers are used to implement the squaring function required. The upper multiplier implements the voltage squaring function, while the lower multiplier implements the current squaring function in order to relate the output and input current, thus simulating power flow correctly.

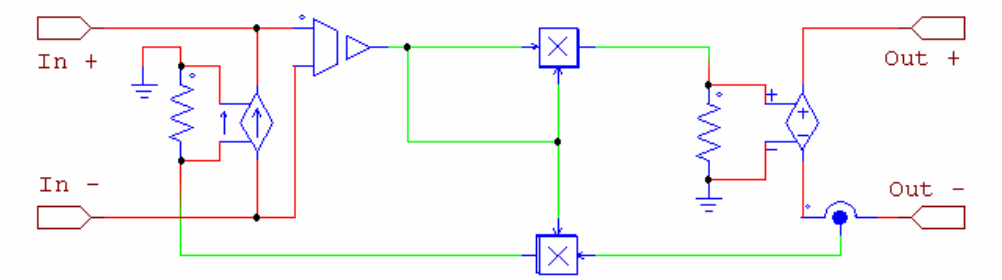


Fig. 4.4 Control Block Detail

Fig. 4.5 shows the result of the simulation, with the red phase voltage and current inputs being in phase. Fig. 4.6 shows the three output phase voltages V_r V_y and V_b summing together to form V_{out}. As can be seen, the output voltage and current are constant, with the output voltage summing to 1½ times the peak input voltage. The results of this preliminary simulation show that the proposed topology can theoretically produce zero output voltage ripple and a unity power factor.

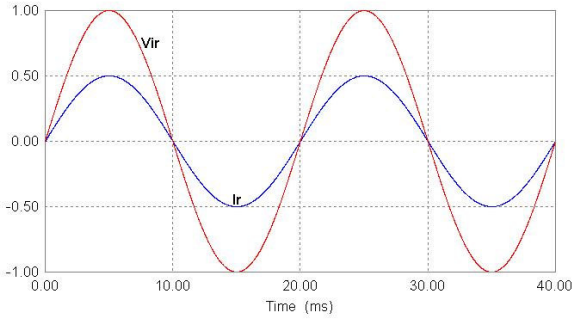


Fig. 4.5 Input Phase Voltage and Current

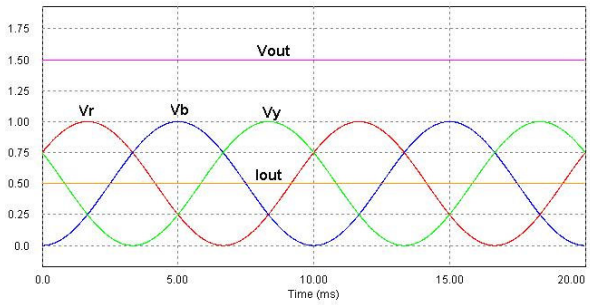


Fig. 4.6 Series Buck Output Waveforms

4.2 Converter Control Features

The proposed three-phase converter topology is shown in Fig. 4.7 with the basic control loops comprising of the pseudo derivative feedback control (PDF) loop (chapter 4.2.2) and the phase locked loop feedforward control (chapter 4.2.1).

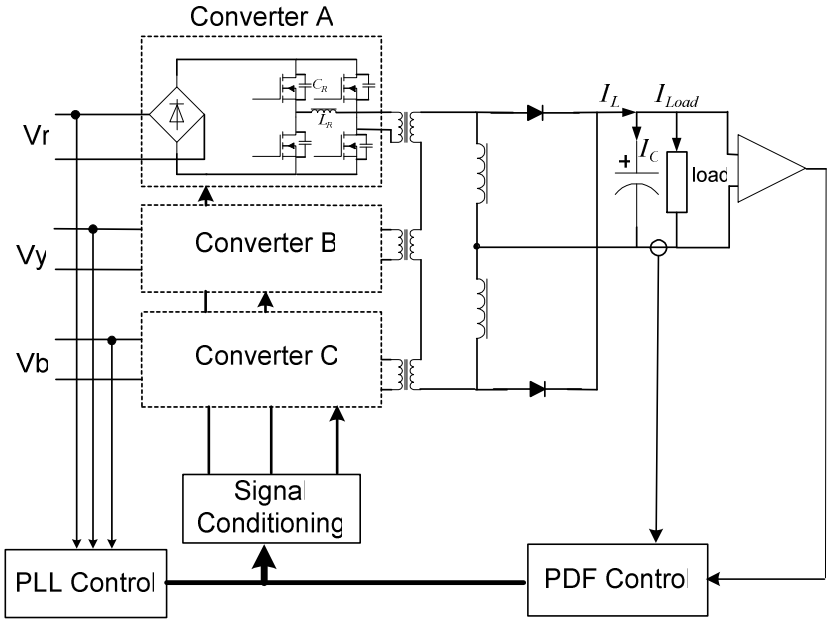


Fig. 4.7 Converter Control Features

4.2.1 PLL Control

In order for the converter system to be able to transfer constant power from source to load, it first needs a mechanism to be able to synchronise with the mains input voltages. Once this is achieved, the desired transfer function can be implemented to produce zero output voltage ripple and unity power factor. A method used to achieve synchronisation with the mains phase voltages is to use a three-phase phase-locked loop (PLL) [1-3]. This allows each converter module to synchronise with its corresponding mains input voltage. The output of the PLL is then an ideal sine wave representation of the input voltage. This output can be used as a reference signal to generate the appropriate squaring function necessary to drive the power converter system.

The proposed converter can be simulated as a closed loop system using a simple PI controller to control the output dc voltage (see Fig. 4.8). The reference voltage is set to a value of 0.8V, since the input phase voltages sum together resulting in a maximum voltage of 1.5V (assuming unity voltages). Therefore, the reference voltage may be set to any value that is less than 1.5V in order to demonstrate regulation.

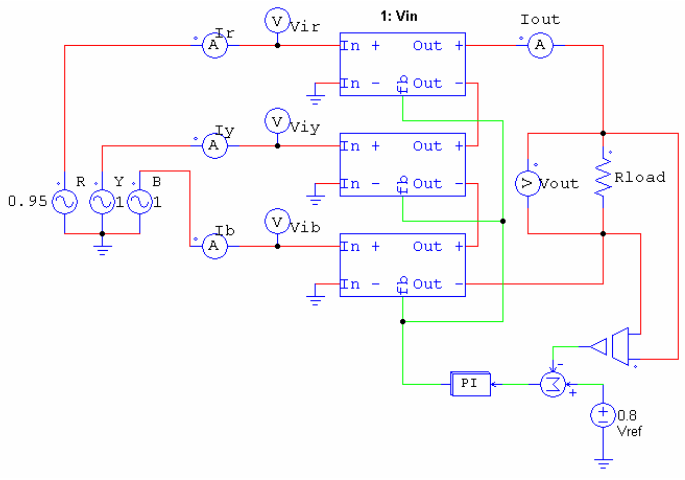


Fig. 4.8 Series Buck Converter with PI control

The feedback control block configuration is shown in Fig. 4.9 with a low pass filter been added with a 2kHz cutoff frequency in order provide a realistic bandwidth.

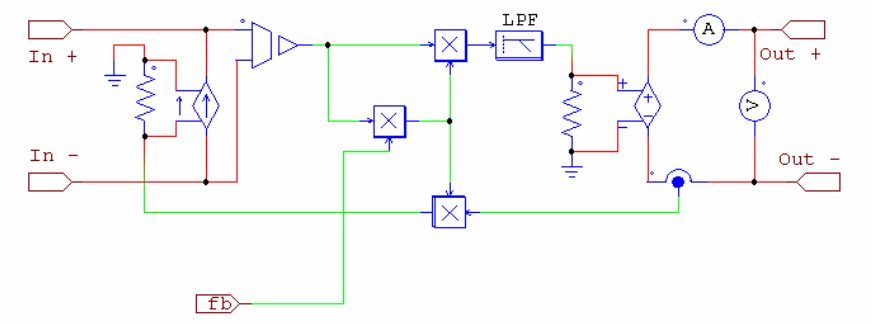


Fig. 4.9 Feedback Control Block

A phase imbalance is applied by forcing the red phase to undergo a 5% decrease from its nominal value at time t=40ms. As a result, output voltage ripple occurs as the outputs are not able to sum to a constant (Fig. 4.10). Under real world conditions, the input voltages are not always ideal, this results in undesirable output voltage ripple.

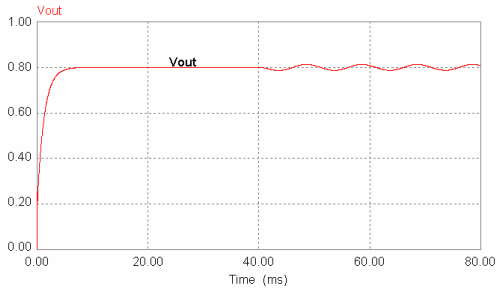


Fig. 4.10 Output Voltage Under Mains Imbalance

Using the PLL, it is possible to provide compensation during mains phase imbalances. A control technique using a three-phase PLL is introduced to the converter system (Fig. 4.11). The PLL block details are seen in Fig. 4.12 with Fig. 4.13 showing details of how the PLL and feedback loops connect into the main control blocks.

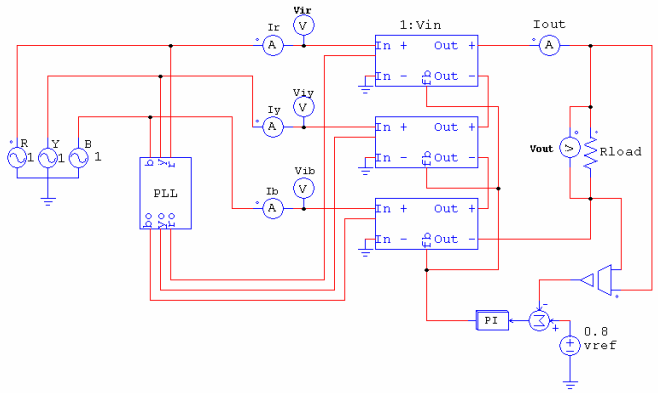


Fig. 4.11 Series Buck Converter with PLL Control

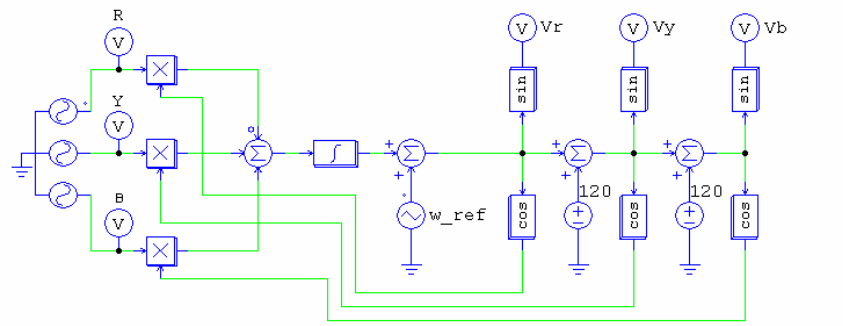


Fig. 4.12 PLL Control Block Detail

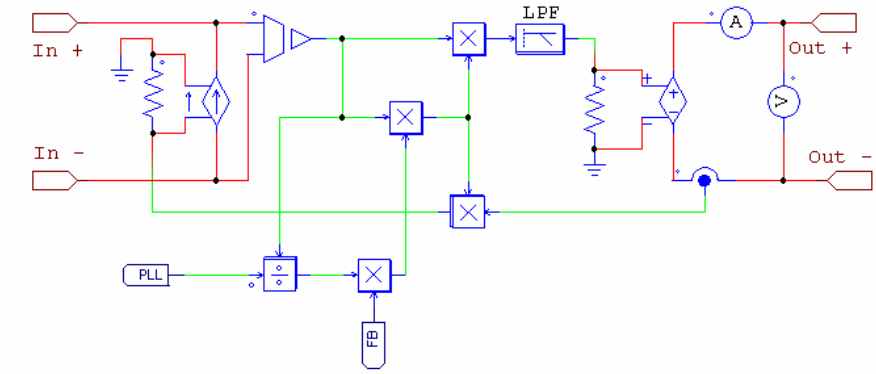


Fig. 4.13 Main Control Bock with PLL and Feedback

The mains red phase is decrease by 5% at t=40ms. It can now be seen from Fig. 4.14, that with PLL control, the output voltage has zero ripple under these conditions. The converter system controller is now able to compensate, given the fact that the PLL is placed in the feedforward path. As the inputs to the PLL are the mains voltages, the outputs of the PLL represent pure sinewaves. These three-phase output signals all have equal magnitude (normalised to unity) and, therefore, provide an ideal representation of the mains voltages. Any discrepancies between the PLL outputs and the mains inputs will show up as a PU error signal. The controller then generates the appropriate compensation signals based on the error, in order to maintain a constant power flow to the load (see Fig. 4.14). This prevents the occurrence of any voltage ripple as a result of mains variations. This approach is used to compensate for voltage transients only, as such having a sustained phase "brownout" will result in output voltage ripple as well as poor power factor. To show this Fig. 4.11 is simulated with phase voltage R set to 0.7V (see Fig. 4.15). This however is not a concern since both the IEC1000-3-2 standard and the psophometric standard is defined only under steady state ideal conditions (i.e. constant load and balanced supply).

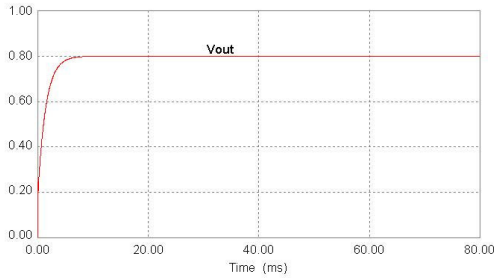


Fig. 4.14 Output Voltage Under Mains Imbalance

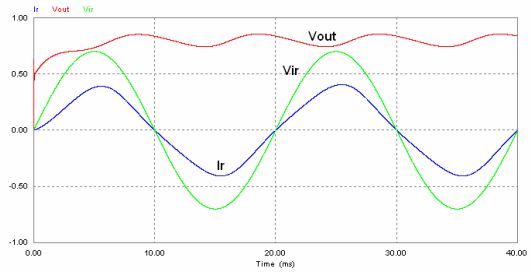


Fig. 4.15 System With Constant Phase Attenuation

4.2.2 PDF Control

It is expected that telecommunication rectifiers are able to provide a constant output voltage under varying loads. It is, therefore, highly desirable to have a system that can respond quickly to load step changes. Pseudo derivative feedback (PDF) control has been used successfully in the area of motion control to offer a high degree of disturbance rejection [4]. This technique can be used to provide an improved response at startup, and during load step changes, in comparison to conventional PI type controllers. The basic PDF feedback control system is shown in Fig. 4.16.

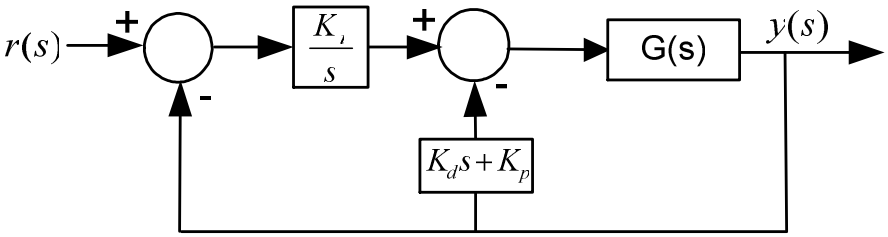


Fig. 4.16 PDF Control Architecture

The closed loop transfer function for the PDF feedback control system is

$$\frac{y(s)}{r(s)} = \frac{K_i G(s)}{K_d G(s) s^2 + s + (K_p + K_i) G(s)} \qquad (1)$$

A typical PI control system is shown in Fig. 4.17

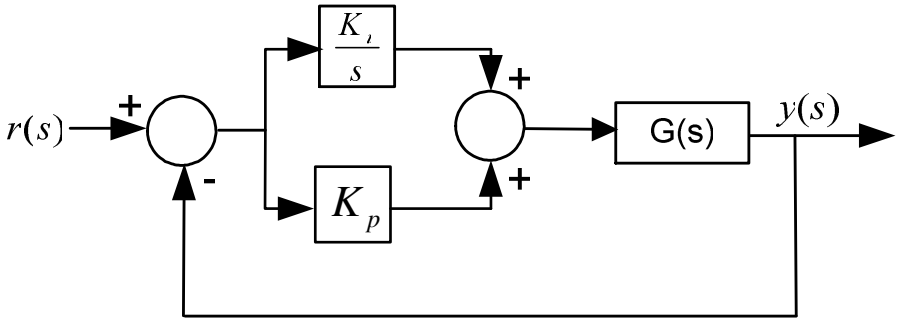


Fig. 4.17 PI Control Architecture

The closed loop transfer function for the PI feedback control system is

$$\frac{y(s)}{r(s)} = \frac{(K_i + K_p s)G(s)}{(1 + K_p G(s))s + K_i G(s)} \tag{2}$$

The PDF control structure in Fig. 4.16 provides all the control aspects of PID control, but without system zeros that are normally introduced by the integral component of a PID controller. This is seen in the characteristic equation (1). A simple PI feedback control system always introduces a zero into the characteristic equation as shown in (2). The name pseudo derivative derives itself from the fact that the rate of the measured parameter is fed back without having to calculate a derivative. This is done by the load current which exhibits rapid change under a step load change. The full system transfer function using PDF control is derived in chapter 7.1. The PDF control system is now simulated on an LC circuit (Fig. 4.18), which represents the output of the buck derived topology used in the project. The details of the rectifier topology are described in chapter 6. The gains were selected to give a realistic output response of a typical second order system under PDF control as is shown in [5] and [6]. Chapter 7 gives a detailed discussion concerning the overall

stability versus gain ratio values. Two different control techniques are simulated; A PDF controller (Fig. 4.18) and a PI controller (Fig. 4.19).

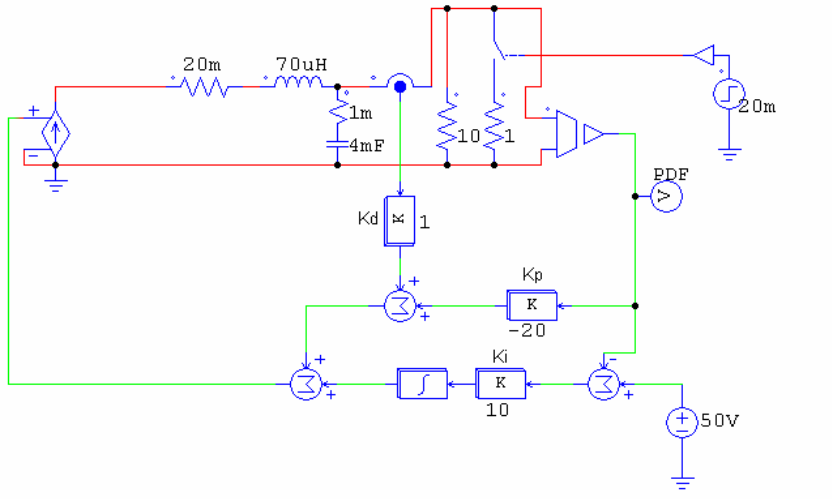


Fig. 4.18 PDF Feedback Control

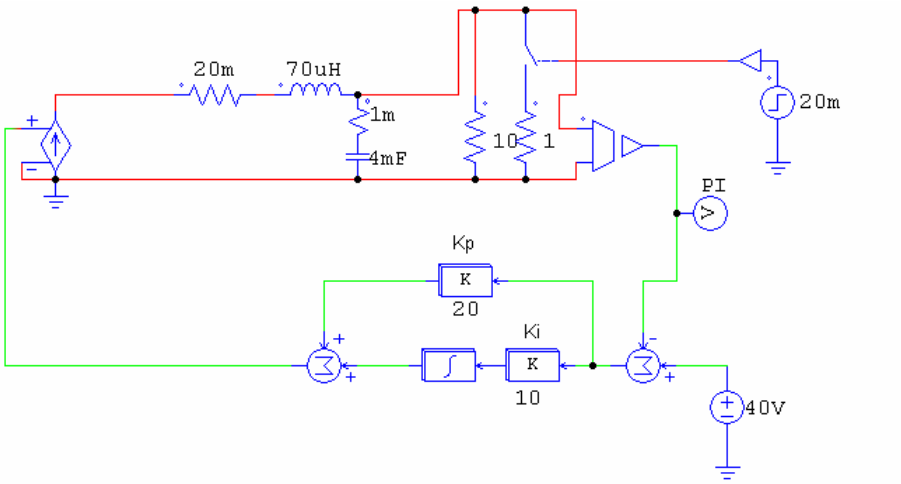


Fig. 4.19 PI Feedback Control

All controllers have the same proportional and integral gains with the PI controller having a 40V reference and the PDF controller having a 50V reference. In a PDF control system, only the integral term exists in the forward path and this is dedicated to eliminating the steady state error.

The remaining terms assigned to the feedback path are used to set the desired closed loop performance such as stability, responsiveness and disturbance rejection (see chapter 7.1). Under a load step change, the PI controller exhibits overshoot, while the PDF controller results in an output response with no overshoot. This is because the load current reacts immediately to any load change and provides a preemptive action that can be used to adjust the controller and provide compensation. Also, the simulations show that the PDF type controller has no startup overshoot, while the PI type controller exhibits startup overshoot. This is because PDF controllers do not contribute to any closed loop zeros and therefore, do not have to be tuned with overdamping to reduce the overshoot as is necessary with PI controllers. The simulated output responses can be seen in Fig. 4.20.

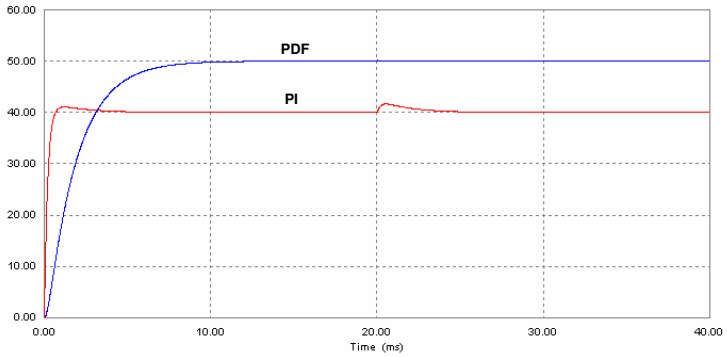


Fig. 4.20 Output Voltages Under Step Load Change

4.3 Summary

A new converter system concept is introduced, consisting of a single-stage design made up of three ideal single-phase buck derived converter modules. The design concept has been shown by simulation to be able to meet with all the expectations of a telecommunication power rectifier system. The design offers benefits over other well known topologies such as simplicity, the ability to independently control each module and thus being able to produce full output power under mains phase transient imbalances. It has also been shown to have the ability to maintain a stable output voltage during a load step change. Accordingly, this topology can be adopted as the basis for the further development of a commercial quality rectifier system. The next chapter describes the details of the implementation of the three-phase PLL controller developed for the control of the proposed new three-phase rectifier.

4.4 REFERENCES

[1] S.K. Chung, “Phase-Locked Loop for Grid-Connected Three-Phase Power Conversion Systems”, IEE Electric Power Applications Conference, Vol. 147, pp. 213-219, May 2000.

[2] S.A.O. de Silva and E.A.A. Coelho, “Analysis and Design of a Three-Phase PLL Structure for Utility Connected Systems under Distorted Utility Conditions”, IEEE Power Electronics Congress, pp. 218-223, Oct. 2004.

[3] S.K. Chung, “A Phase Tracking System for Three-Phase Utility Interface Inverters”, IEEE Transactions on Industrial Electronics, Vol. 15, pp. 431-438, May 2000.

[4] J.K. Kang, J.T. Lee, Y.M. Kim, B.H. Kwon, K.S. Choi, “Speed Controller Design For Induction Motor Drives Using a PDF Control and Load Disturbance Observer”, International Conference on Industrial Electronics, Control and Instrumentation, Vol. 1, pp. 799-803, Oct. 1991.

[5] D.Y. Ohm, “Analysis of PID and PDF Compensators for Motion Control Systems”, IEEE Industry Applications Society Annual Meeting, Vol. 3, pp. 1923-1929, Oct. 1994.

[6] D. Xue and D.P. Atherton, “A Reduction Based PDF Controller Design Algorithm for a Class of Plant Models”, IEEE Decision and Control Conference, Vol. 3, pp. 2917-2922 Dec. 1993.

5 PHASE-LOCKED LOOP

This chapter describes the three-phase phase-locked loop (PLL) developed for the control of the power converter prototype. It highlights the unique difference between the proposed method and traditional three-phase PLL approaches, which require coordinate transformations. A detailed description is given of the PLL structure with mathematical modelling and simulations showing the predicted performance of the system. The PLL is implemented on a TMS320F2812 digital signal processor and a performance analysis is conducted and the results discussed.

The PLL was originally described in 1923 and 1932 [1]. It has been used as a common way of recovering and utilising phase and frequency information in electrical systems. In the area of power electronics, the PLL technique has been adopted in the speed control of electric motors. This technique allows for the synchronising of utility voltages and the control of currents or voltages in utility interface operations [2]. A commonly used three-phase PLL structure is illustrated in Fig. 5.1. In this design, the phase voltages V_a,V_b, and V_c are obtained from the line voltages. These stationary reference frames are transformed via the Clark-Park transformation [3-4] into a reference frame synchronised to the utility frequency. The angle θ used in these transformations is obtained by integrating a frequency command ω^*. If the frequency command is identical to the frequency of the utility ω_{ref}, the voltages V_d and V_q appear as dc values depending on the angle θ. Setting the direct axis reference voltage (V_d^*) to zero, results in the extinguishing of the error between V_d^* and V_d due to the feedback. This locks the PLL output with the utility voltage. In order to generate three-phase outputs (u,v,w), θ needs to undergo an inverse Park and inverse Clark transformation.

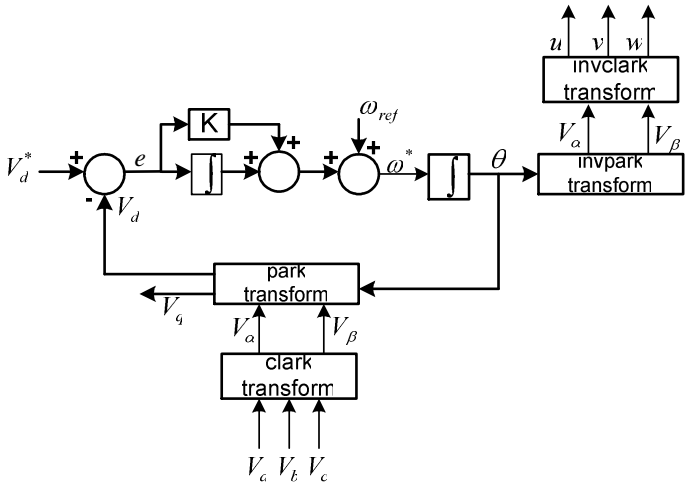


Fig. 5.1 Traditional PLL Structure

5.1 New PLL Structure

A new three-phase PLL structure is introduced and shown in Fig. 5.2. Unlike the traditional design, the new PLL operation does not involve any co-ordinate system transformations. This results in a more simple PLL solution.

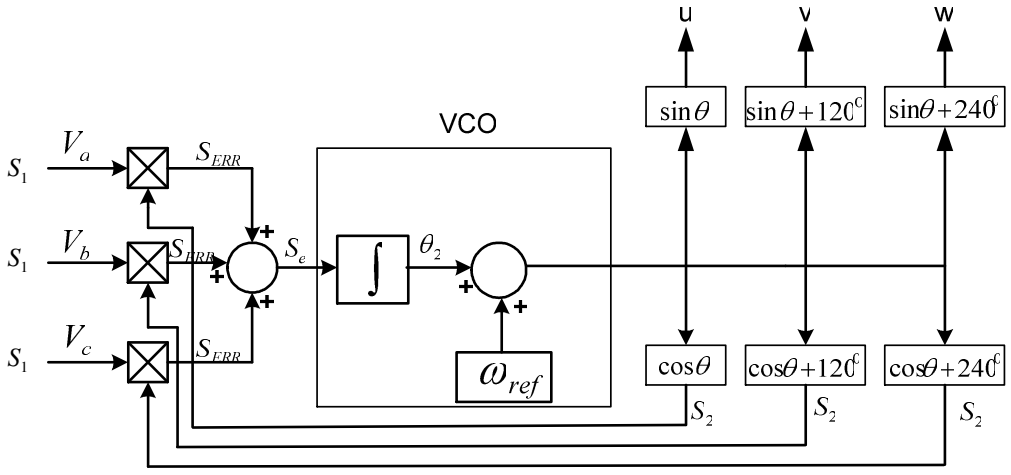


Fig. 5.2 New Proposed PLL Structure

The PLL consists of the input three phase voltage signals, V_a, V_b, V_c, being fed directly into multipliers. These multipliers serve as phase detectors. In any PLL system, under conditions of a phase lock, the two input signals into the multiplier are phase shifted by 90°. The principle of phase detection is shown in the following mathematical analysis; where S_1 and S_2 are two sinusoidal signals phase shifted by 90° and S_3 is their product.

$$S_3(t) = S_1(t)S_2(t)$$

where $S_1(t) = A_1 \sin[\omega t + \theta_1(t)]$

and $S_2(t) = A_2 \cos[\omega t + \theta_2(t)]$

The output of the multiplier is

$$S_3(t) = A_1 A_2 \sin[\omega t + \theta_1(t)]\cos[\omega t + \theta_2(t)] \quad (1)$$

This expression can be rewritten as

$$S_3(t) = \frac{A_1 A_2}{2}\sin[\theta_1(t) - \theta_2(t)] + \frac{A_1 A_2}{2}\sin[2\omega t + \theta_1(t) + \theta_2(t)] \quad (2)$$

In this form, it can be seen that the multiplier signal consists of two parts; the first being a function of the phase difference only; and the second with a frequency at twice the signal frequency plus the sum of the two phases. In other words, the multiplier output consists of a second harmonic signal with a dc offset which is not a function of frequency but of the phase difference. The first term is called the error signal $S_{err}(t)$.

$$S_{err}(t) = \frac{A_1 A_2}{2}\sin[\theta_1(t) - \theta_2(t)] \quad (3)$$

If the phase difference is zero degrees, then the error signal is zero. This represents the locked state of the PLL. Any state other than the locked state will result in a non-zero error signal. In

single-phase PLL systems, it is necessary to remove the second harmonic term by using a low pass filter, as it contains no useful information.

In the proposed three-phase PLL, this second harmonic term does not naturally occur and, therefore, reduces the filtering requirement of the system. If the output signal of each multiplier shown in Fig. 5.2 is represented by equation (1), but phase shifted by 120°, then the following mathematical analysis applies.

$$\text{Let } \frac{A_1 A_2}{2} = G \text{ and } [2\omega t + \theta_1(t) + \theta_2(t)] = \varphi \tag{4}$$

The second harmonic term can now be simply written as $G\sin\varphi$. In the proposed PLL, the outputs of the phase detectors are summed together, and under conditions of a phase lock the resulting error signal or dc term will be zero.

$$G\sin\varphi + G\sin(\varphi + 120^o) + G\sin(\varphi + 240^o)$$

$$= G\sin\varphi - \frac{1}{2}G\sin\varphi + \frac{\sqrt{3}}{2}G\cos\varphi - \frac{1}{2}G\sin\varphi - \frac{\sqrt{3}}{2}G\cos\varphi$$
$$= 0$$

Hence, under ideal mains conditions there is theoretically no second harmonic component present. This result reduces the filtering effort required for implementation. Similarly, any common noise at the three-phase inputs will also be removed. Each multiplier output has a sinusoidal signal $S_{ERR}(t)$, which is summed together to give

$$S_e(t) = \frac{3A_1 A_2}{2}\sin[\theta_1(t) - \theta_2(t)] \tag{5}$$

Equation 5 represents the dc error signal which is integrated and used to shift θ_2 to the same value as θ_1. If the phase difference is zero degrees then the error signal $S_e(t)$ is zero, which is the desired lock state of the PLL.

In general, the voltage controlled oscillator (VCO) has a constant K_{vco} representing the VCO gain factor which is calculated by determining the output of the VCO in response to an error signal (see Appendix B).

The feedback signal out of the VCO for each phase is given by

$$S_2(t) = A_2 \cos[\omega_{ref} + \theta_2(t)] \tag{6}$$

Since the error signal S_e sets the VCO frequency and phase is the integral of the frequency over time, the phase of the feedback signal can be written as

$$\theta_2(t) = 2\pi K_{vco} \int_0^t S_e dt \tag{7}$$

$$= 2\pi K_{vco} S_e t$$

As long as the error signal has a non-zero value, the phase of the VCO signal $\theta_2(t)$ will keep on increasing until such time as it equals $\theta_1(t)$, and the error decreases to zero. Accordingly, substituting equation (7) into (5) $S_e(t)$ can now be represented as

$$S_e(t) = \frac{3A_1A_2}{2} \sin[\theta_1(t) - 2\pi K_{vco} \int_0^t S_e dt] \tag{8}$$

The equation of S_e can be linearised by making the following assumptions.

$\sin(\theta) \approx \theta$ for small θ

$$\sin[\theta_1(t) - \theta_2(t)] \approx [\theta_1(t) - \theta_2(t)]$$

Now (8) can be rewritten by removing the sin function

$$S_e(t) = \frac{3A_1A_2}{2}[\theta_1(t) - 2\pi K_{vco}\int_0^t S_e dt]$$

$$S_e(t) = \frac{3A_1A_2}{2}[\theta_1(t) - 2\pi K_{vco}S_e t] \quad (9)$$

It can now be seen that, at time t, the frequency of the signal produced by the VCO increases by $K_{vco}S_e$. As long as the error signal is present, the phase keeps changing linearly. However, as the phase of the signal out of the VCO changes, the new difference in phase decreases and the error signal amplitude decreases as a consequence. This decreases the phase change further, until the error signal amplitude has reached zero. In the event of a negative error signal the VCO will simply decrease its frequency by $K_{vcoo}S_e$ at time t giving the effective frequency range as

$$\omega_{out} = \omega_{ref} \pm K_{vco}S_e \quad (10)$$

5.2 Discrete PLL Model

Since the PLL is to be implemented on a DSP, an analysis of the discrete operation is performed. A discrete model of the analogue equivalent shown in Fig. 5.2 is represented by Fig. 5.5.

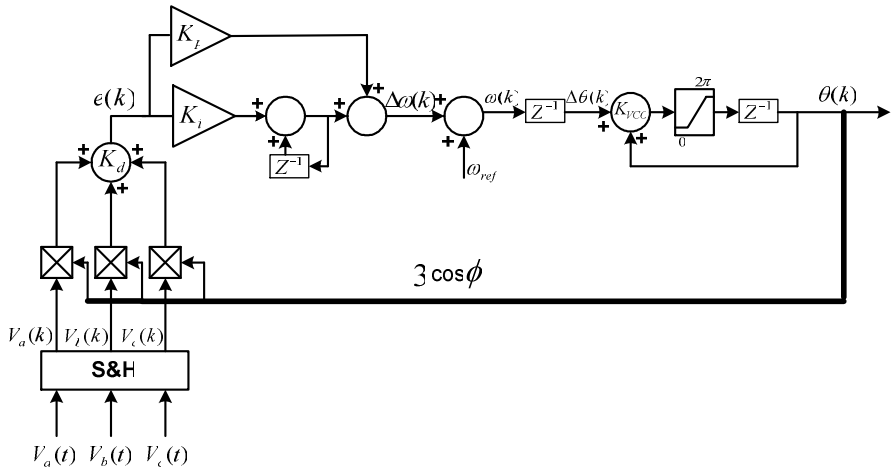


Fig. 5.5 Discrete PLL Model

The three-phase inputs after being sampled by the digital signal processor (DSP) are represented as

$$V_a(k) = 1PU\sin(\theta(k))$$
$$V_b(k) = 1PU\sin(\theta(k) + 2\pi/3)$$
$$V_c(k) = 1PU\sin(\theta(k) - 2\pi/3)$$

Where PU represents per unit.

The multipliers serve as phase detectors, with the phase error in each phase being summed together resulting in a dc error signal *e(k)*. This error signal is fed into the proportional-integral controller of the PLL, and used to calculate the change in angular frequency of the mains voltage $\Delta\omega(k)$.

$$\Delta\omega(k) = \left(K_p + \frac{K_i z}{z-1}\right)e(k)$$

The reference angular frequency $\omega_{ref}=2\pi f$ (where f is the reference frequency 50Hz), is added to $\Delta\omega(k)$.

$$\omega(k) = \Delta\omega(k) + \omega_{ref}$$

Multiplying $\omega(k)$ by the sampling time, which is represented by unit delay z^{-1}, determines the sampling time increment of the phase angle $\Delta\theta(k)$.

$$\Delta\theta(k) = z^{-1}\omega(k)$$

By integrating the increment $\Delta\theta(k)$ over the range 0-2π, the estimated phase angle of each three-phase mains phase voltage $\theta(k)$ is obtained.

$$\theta(k) = \frac{z\Delta\theta(k)}{z-1} \tag{11}$$

The cosine functions of the estimated angle in (11) are fed back into the phase detectors and used to drive the error signal towards zero, resulting in the elimination of the angle between the PLL outputs and the grid phase angle.

5.3 Discrete PLL Control Model

A control model of the PLL is needed for analysis purposes in order to determine the expected performance characteristics, once implemented on a DSP controller. By assuming the phase error is kept within a limited range, the PLL can be modelled as a linear system. This is a reasonable assumption, since PLLs are normally only operated within their locking range, as beyond this, instability results [5]. A linearised discrete PLL model can be represented as in Fig. 5.6.

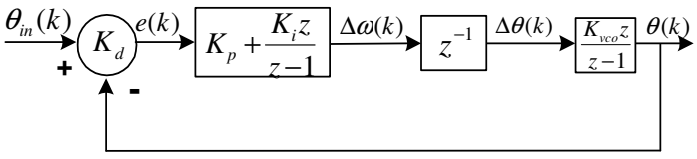


Fig. 5.6 Linearised Discrete Model

In Fig. 5.6, K_p and K_i represent the proportional and integral gains and z^{-1} represents a sample delay. In addition, K_d is the phase detector gain. It determines the phase detector output in

response to a phase error. K_{vco} is the gain of the VCO. The discrete closed loop transfer function can now be derived by firstly multiplying all the blocks together as follows:

$$G(z) = K_{vco}K_d\left[\frac{(K_p + K_i)z - K_p}{(z-1)^2}\right] \tag{12}$$

The closed loop transfer function H(z) for the system is by definition given as

$$H(z) = \frac{G(z)}{1+G(z)} \tag{13}$$

Substituting (12) into (13) one obtains

$$H(z) = \frac{(K_{vco}K_dK_p + K_{vco}K_dK_i)z - K_{vco}K_dK_p}{z^2 + (K_{vco}K_dK_p + K_{vco}K_dK_i - 2)z + (1 - K_{vco}K_p)} \tag{14}$$

For equation simplicity, we set $K_{vco}K_dK_p=\alpha$ and $K_{vco}K_dK_i=\beta$. The closed loop transfer function of Fig. 5.6 can now be written as

$$H(z) = \frac{(\alpha+\beta)z - \alpha}{z^2 + (\alpha+\beta-2)z + (1-\alpha)} \tag{15}$$

5.4 Loop Stability

A digital PLL is stable if all of its poles are inside the unit circle, and unstable if any pole lies outside the unit circle. One of the most efficient criteria for testing the stability of a discrete-time system is Jury's stability criteria [6]. For a second order system, according to this criterion, the necessary and sufficient conditions for stability are

$\Delta(1)>0$
$\Delta(-1)>0$
$|k_0|<k_2$

where Δ is the characteristic equation of the second order system or the denominator of the transfer function in (15) which is rewritten as

$$\Delta(z)=k_2 z^2+k_1 z+k_0 \qquad (16)$$

By applying the Jury stability conditions to (16), stability is obtained when

$0<\alpha<2$ and $0<\beta<4-2\alpha$

Consider now a step change in the phase of the incoming signal, which can be shown as

$$\theta_{in}(t) = u(t)\Delta\theta_{in}$$

u(t) is the unit step function and $\Delta\theta_{in}$ is the size of the input phase step. The instantaneous phase has jumped from its old value to a new value by $\Delta\theta_{in}$. In the z domain, this can be expressed as

$$\theta_{in}(z) = \frac{\Delta\theta_{in} z}{z-1}$$

and the phase error transfer function E(z) for a digital system can be expressed as

$$E(z) = \left[1 - \frac{\theta(z)}{\theta_{in}(z)}\right]\theta_{in}(z)$$

Substituting (14) into E(z) gives

$$E(z) = \frac{\Delta\theta_{in} \bullet z(z-1)}{z^2 + (\alpha+\beta-2)z + (1-\alpha)}$$

Applying the final value theorem to E(z)

$$\lim_{k\to\infty} e(kt) = \lim_{z\to 1} \frac{\Delta\theta_{in}(z-1)^2}{z^2 + (\alpha+\beta-2)z + (1-\alpha)} \tag{17}$$

Setting z=1, it can be seen that the expression becomes zero, thus proving that the error signal over time will go to zero in response to a step phase change at the input. Further analysis shows similar results under conditions of a frequency step and a frequency ramp [7].

In order to fully make use of the transfer function, one needs to determine the relevant gain coefficients. The phase detector gain is defined as the slope of the output calculated as cycles^{-1}. This was determined to be K_d=0.978cycles^{-1} as described in [8] and can be found in Appendix B. The VCO gain is the change in output frequency in response to an error signal and is calculated to be K_{vco}=0.099cycles [8].

The following time continuous approximation can be made for a digital system, as discussed in [7].

$$\varsigma \approx \frac{1}{2}\sqrt{\frac{K}{K_i}} \tag{18}$$

where

f_s= sampling frequency

K=loop gain= $K_d K_{vco} K_p$ where K_p=proportional gain

ζ=damping factor

ω_n=natural frequency

K_i=integral gain

The PLL is chosen to have a damping factor of 0.707, as this should allow only one overshoot in the transient response and it is well known to be the optimum damping factor value for a second order system. Choosing values of K_p=22 and K_i=1 will give ζ=0.707 according to (18). The same ratio could be found by using a range of gain values, however very large values would result in fewer iterations taking place before the upper and lower limit thresholds in the digitized PLL are reached, and as such the error is not able to be reduced to zero thus degrading the PLL performance. Applying these values, as well as the known values for K_{vco} and K_d, to the transfer function in (15) gives the closed loop transfer function in the z domain represented by H(z) as

$$H(z) = \frac{0.094z - 0.09}{z^2 - 1.906z + 0.91} \tag{19}$$

5.5 Simulated PLL Responses

The transfer function (21) has been simulated using a software package called PSIM. The input step response and the frequency and phase responses are shown in Figs. 5.7 and 5.8 respectively.

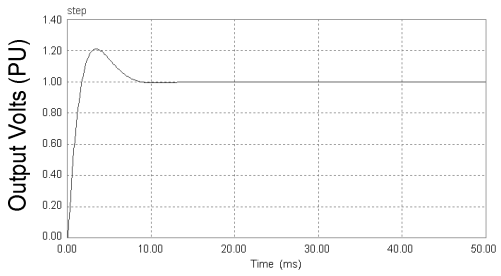


Fig. 5.7 PLL Input Step Response

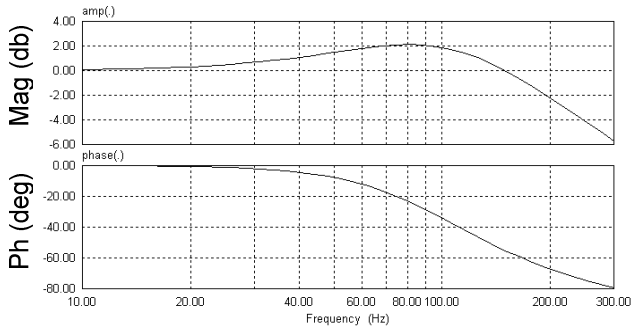


Fig. 5.8 PLL Frequency and Phase Response

From the simulations, it can be seen that the input step response (Fig. 5.7) yields a settling time of 8ms. The frequency response plot of gain (decibels) vs frequency (Hertz) (Fig. 5.8) shows that the PLL has a -3db crossover frequency of 149Hz. The system is shown to have a phase margin of 126˚ indicating a stable system. It can also be seen from the frequency response graph that there is some gain peaking. This is due to the fact that there is always a zero in the numerator of the transfer function, even though the spacing between the zero and the closest pole decreases with increasing damping, but the pole never actually coincides with the zero. Accordingly, a second order PLL will always exhibit some peaking.

In order to verify the limits of the Jury stability criteria the system is simulated with $\alpha=3$ which is set outside the stability limits. The results are shown in Fig. 5.9 where the system is clearly oscillating thus verifying the stability limits set by the Jury stability test.

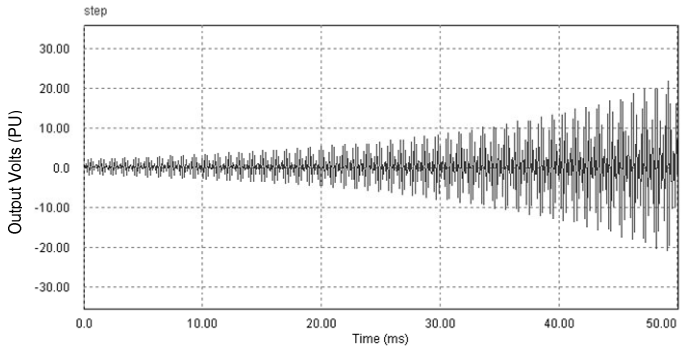


Fig. 5.9 PLL Input Step Response

5.6 PLL Performance

The digital implementation of the software PLL has been tested on a TMS320F2812 DSP with a 10 kHz sampling frequency. Fig. 5.10 shows a block diagram of the PLL implementation on the DSP. A three-phase function generator produces the input signal voltages. The on-board A/D converters sample these input signals and, consequently, the PLL outputs the generated phase signals via the PWM ports. The performance of the PLL is tested under various conditions of input step changes as well as for non-ideal mains voltages as described in sections 5.6.1 and 5.6.2 respectively.

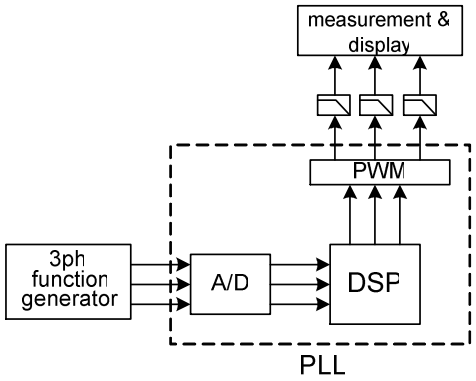


Fig. 5.10 PLL Digital Implementation

5.6.1 PLL Transient Response

The PLL dynamics are tested with the aim of observing its ability to obtain phase lock under various transient conditions. A startup response is investigated by starting the PLL while the three-phase generated mains are applied to the inputs. The response of the red phase is shown in Fig. 5.11. The PLL at startup has 180˚ phase shift with respect to the main phase voltage, the PLL achieves a lock and begins to track the mains within 10ms.

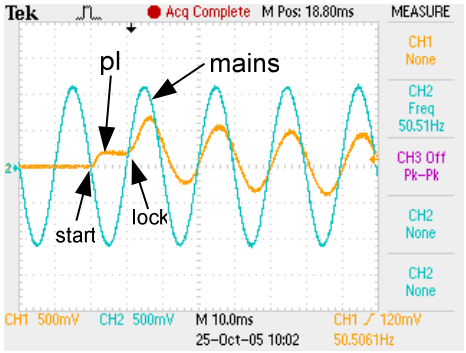


Fig. 5.11 PLL Startup Response

In Figs. 5.12 and 5.13, the PLL is tested under conditions of phase angle jumps. This is achieved by causing the PLL to undergo a sudden phase angle change by resetting the VCO at the appropriate time and observing the time taken to resynchronise. The response of the PLL to a phase angle jump of 90˚ is shown in Fig. 5.12. It can be seen that the PLL is able to recover from the disturbance and regain tracking after 7ms. Fig. 5.13 shows that, in the worst case, an 180˚ phase angle jump, the PLL regains synchronism in 10ms. The PLL output signals are generated by the PWM ports at a frequency of 10kHz. Accordingly, in order to see the output waveforms on the oscilloscope, the PWM signals need to be filtered to remove the switching harmonics. As a

consequence of passing the PWM signals through a passive low pass filter having a 129Hz cutoff frequency, there is a 21° phase shift introduced between the mains and PLL traces.

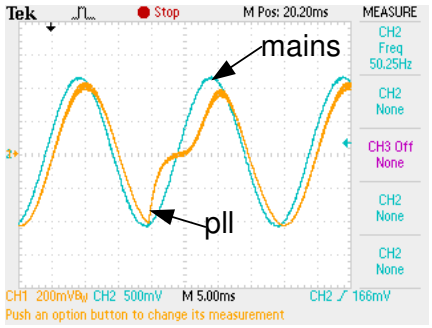


Fig. 5.12 PLL Under 90^0 Phase Angle Jump

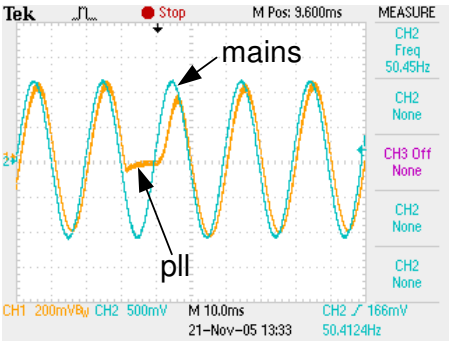


Fig. 5.13 PLL Under 180° Phase Angle Jump

5.6.2 PLL Under Distorted Mains Voltages

In reality, the mains voltage is not a pure sinusoid. It can be distorted by various non-linearities, such as phase imbalances and line harmonics. The PLL is tested by subjecting it to non-ideal mains conditions such as flat topping and 3rd harmonic distortion. The generated mains signals have been passed through the same filter as the PWM outputs in order to show phase lock. The system is subject to flat topping on all mains phases with Fig. 5.14 showing one phase of the mains

voltage and the corresponding PLL output. A three-phase signal with 3rd harmonic distortion is applied to the PLL, the corresponding input and output are seen in Fig. 5.15

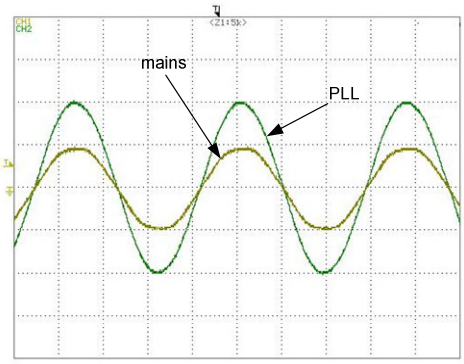


Fig. 5.14 PLL Under Mains Flat Topping

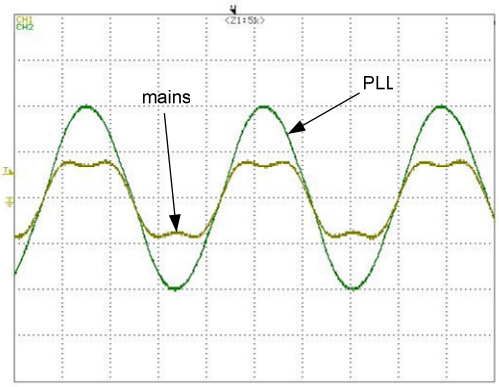


Fig. 5.15 PLL Under Mains Harmonic Distortion

The phase locked loop is able to maintain phase lock over a theoretical range from 0Hz to 100Hz. This is known as the hold range. The lock range, defined as the frequency range over which acquisition can be made within a single beat note was found to range from 35Hz to 75Hz.

The power converter is expected to operate under much less extreme mains conditions, as defined by the EN50160 power quality standard [8], which allows for just a ±10% magnitude variation. The PLL, therefore, is expected to maintain control of the converter under these conditions.

5.7 Conclusion

A novel software three-phase PLL has been introduced and a system model transfer function derived. Tests have shown that the PLL is able to recover from a worst case phase angle jump, and regain synchronism within half a mains cycle or 10ms. Simulations of the transient response show a settling time of around 8ms with one overshoot. Simulations also show a natural frequency of 149Hz, with a phase margin of 126°, thereby indicating that the PLL is inherently stable.

Under distorted mains conditions, the PLL is able to maintain phase lock and produce a clean output waveform. The PLL has been demonstrated to produce a very good filtering action with the ability to naturally remove all common phase distortions. This allows the PLL system to comprise both excellent noise rejection and a high degree of robustness.

5.8 REFERENCES

[1] H. Awad, J. Svensson, and M.J. Bollen, "Tuning Software Phase-locked Loop for Series-Connected Converters", IEEE Transactions on Power Delivery, Vol. 20, No. 1, pp. 300-308, Jan. 2005.

[2] S.K. Chung, "A Phase Tracking System for Three Phase Utility Interface Inverters", IEEE Transactions on Power Electronics, Vol. 15, No. 3, pp. 431-438, May 2000.

[3] S.K. Chung, "Phase-Locked Loop for Grid-Connected Three-Phase Power Conversion Systems", IEE Transactions on Electric Power Applications, Vol. 147, No. 3, pp. 213-219, May 2000.

[4] L.N. Arruda, S.M. Silva and B.J.C. Filho, "Pll Structures for Utility Connected Systems", IEEE Transactions on Industrial Applications, Vol. 4, pp. 2655-2660, Oct. 2004.

[5] L. Xiu, W. Li, J. Meirs, and R. Padakanti, "A Novel All-digital PLL with Software Adaptive Filter", IEEE Journal of Solid State Circuits, Vol. 39, No. 3, pp. 476-483, March 2004.

[6] B.C. Kuo, "Automatic Control Systems," 7th ed., Prentice Hall, 1994.

[7] F.M. Gardner, "Phaselock Techniques", 3rd ed., Wiley, NY, 2005.

[8] Voltage Characteristics of Electricity Supplied By Public Distribution Systems EN50160:2000

6 RECTIFIER CONTROL

Eaton Power Quality Ltd. has had a long association with resonant topologies and was one of the first companies to use them commercially. Thus, given the experience gained it was decided the proposed three-phase rectifier is to be in the form of the full bridge zero voltage switched (ZVS) phase-shifted current doubler topology. The use of ZVS is well known and has several advantages over non-resonant topologies including; lossless switching transitions; reduced EMI/RFI at the transitions; no power loss due to discharging of the output capacitance; and the ability to incorporate parasitic components as part of the resonant circuit [1-3]. In addition, the gate drive requirements are reduced in a ZVS design. This is due to having no gate to drain (Miller) charge, which occurs when the drain-source voltage equals zero. Primarily, ZVS is appropriate with high frequency switching operation where, under normal circumstances, rapid charging and discharging of the semiconductor switch capacitance would represent substantial power loss. This chapter discusses the topology of the converter in detail, as well as the interface circuitry and DSP control implementation. An analysis of the complete digital control methodology, which supports the prototype, is also provided.

6.1 Topology

The converter prototype uses a series LC resonant tank. The resonant frequency was calculated by using the following formula:

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

Where f_r = resonant tank frequency, L_r =resonant inductance, C_r =resonant capacitance

The resonant capacitance is calculated by considering the MOSFET output capacitance (parasitic) C_{OSS}. This is multiplied by a factor of $\frac{4}{3}$ as per the MOSFET manufacturer's application notes in order to approximate the correct average capacitance value with a varying drain voltage. During each transition, two switch capacitances are driven in parallel, doubling the total capacitance to $\frac{8}{3}C_{OSS}$. The transformer capacitance C_{XFMR} must also be added as this is not negligible. The resonant capacitance, C_r:

$$C_r = \frac{8}{3}C_{OSS} + C_{XFMR} \qquad (2)$$

$$= \frac{8}{3} \bullet 900\times10^{-12} + 15\times10^{-12}$$

$$=2.4\text{nf}$$

The resonant inductance is made up of the series link resonant inductor L_R plus the combined parallel inductances of the leakage inductance L_{LKG}, and the magnetizing inductance L_{MAG}. The resonant inductance was calculated as follows:

$$L_r = L_R + L_{LKG} // L_{MAG} \text{ where } L_{LKG} = 1.56\times10^{-6}\,\text{H and } L_{MAG} = 0.85\times10^{-3}\,\text{H} \qquad (3)$$

$$= 0.5\times10^{-6} + 1.56\times10^{-6}$$

$$=2.06\mu\text{H}$$

In order for resonance to take place at light loads, there needs to be enough inductive energy to drive the resonant capacitors to the opposite supply rail. This transition needs to take place within the allocated transition interval.

The resonant frequency is calculated by using (1) and is found to be 2.26MHz. The resonant tank period T_r must be at least four times higher than the time t_{MAX} required to discharge the parasitic capacitances at light load (transition interval).

$$T_r = 4t_{MAX}$$

$$t_{\max} = 111ns$$

This is the time between the turning off of the upper MOSFET in a leg until the turning on of the lower MOSFET in the same leg or visa versa. The maximum transition time selected requires the maximum effective duty cycle to be limited to 97%. A series resonant converter operates with a step-down voltage conversion ratio and is, therefore, best suited for the particular application. The reason for using a full bridge design is that the transformer primaries need to be short-circuited during the off time when that particular bridge is not transferring power to the load. Without this function, the transformer would present a high impedance point and, due to the series connection of the three secondary windings of the transformers, would limit the flow of power to the load. A current doubler topology was chosen, as it presents a convenient way in which to connect the three transformer secondary windings together, while still maintaining a buck derived topology (see Fig. 6.1).

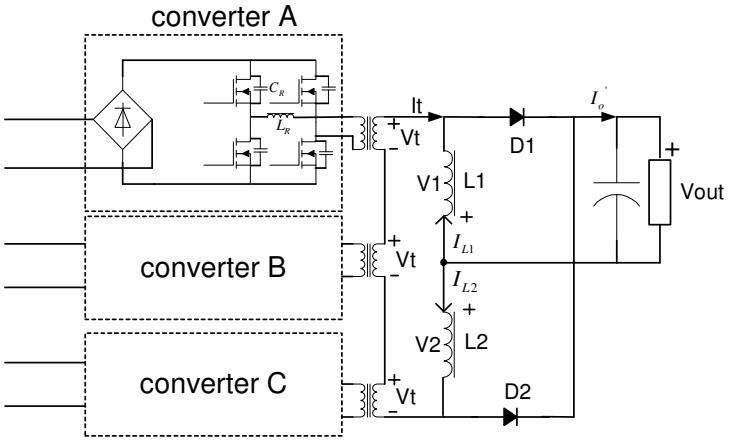


Fig. 6.1 Rectifier Topology

The output voltage is controlled by having both halves of the bridge network in each converter operating at a 50% duty cycle. The phase shifting between the diagonal switches in the right and left legs of the bridge sets up the duty cycle that generates the required output voltage.

6.1.1 Current Doubler

During the first active period the voltage across the transformer secondary windings Vt is positive, since each converter switches on at the same time (see Fig. 6.1). Current flows in positive direction in both filter inductors, L1 and L2. During this period D1 is forward biased while D2 is kept off by Vt. The current path for L1 runs through D1 and the output capacitor and does not flow through the secondary winding of the transformers. The current of the second filter inductor L2 flows through the transformer winding and D1, closing the loop through the output capacitor. Hence the output current is the sum of the DC components of the two filter inductor currents; the transformer sees only half of the load current during the active time interval.

During this time the voltage across L1 is negative and equals the output voltage causing the current in L1 to decrease. On the other hand, the voltage across L2 is positive, causing the current in L2 to

increase. The active period is followed by a free-wheeling interval. Vt is not present across the secondary winding during this period. The voltage across L2 becomes negative and equal to the output voltage thus producing a negative slope in the current through L2 which continuous to flow through the transformer secondary windings. The conditions for L1 do not change. At the beginning of the next active interval, a negative voltage appears across the transformer secondary windings. D1 is turns off while D2 is forward biased. The current rapidly changes direction in the transformer windings and is equal to the current of L1. The current of L2 is no longer flowing through the transformer secondary windings and decreases at a rate determined by the inductance and the output voltage. Having a positive voltage across L1, the current starts to build up in the inductor. The full operating cycle is completed by another free-wheeling period when Vt across all the secondary windings become zero. The negative output voltage Vout appears on L1 causing its current to decrease with no change in the state of L2. Fig. 6.2 shows the typical waveforms of a current doubler. It is assumed for simplicity that the three converter modules each have the same on time, thereby having Vt the same.

The current doubler topology is advantageous in that no centre tap transformer is required however, there is no outright advantage over a full bridge topology since even though there are two output inductors each only carries half of the output current, so the total inductor volumetric size is the same as that of a full bridge. In addition the output diodes also have to block twice the input voltage reflected through the transformer turns ratio as in a full bridge topology.

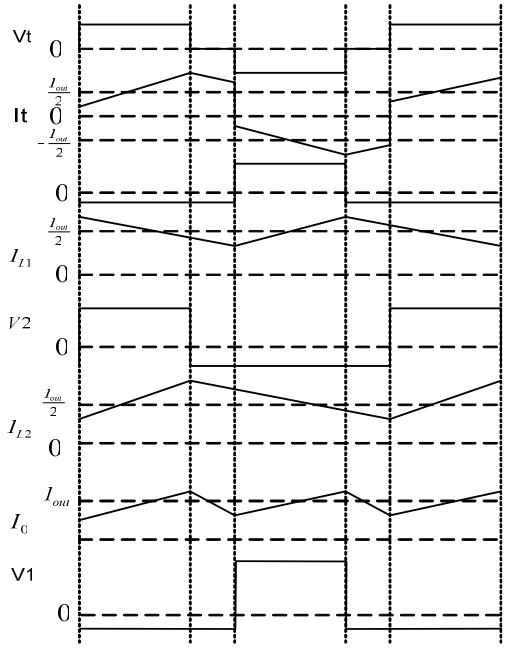
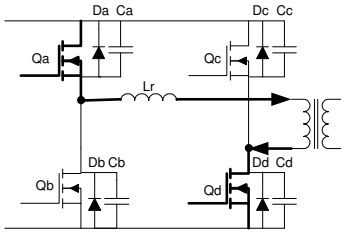


Fig. 6.2 Current Doubler Waveforms

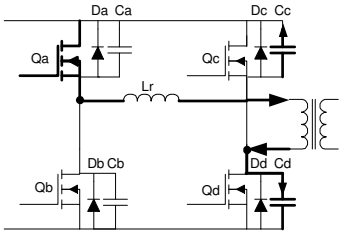
6.1.2 ZVS Switching

The mechanism of ZVS operation in a full bridge circuit utilising phase shift control is described in detail in this section. Assuming initial conditions, having transistors Qa and Qd on, as shown in (6.3a), the instant switch Qd is turned off by the control circuitry the resonant transition of the right hand leg begins. The drain-source capacitance shown in figures 6.3 refers to the parasitics present in the MOSFET, and the diodes represent the MOSFET body diode. When switch Qd is turned off, the primary current continues to flow and charges up the capacitance of Qd from zero volts to the upper rail voltage. Simultaneously, the output capacitance of Qc is discharged. This resonant transition leaves Qc with no drain to source voltage prior to turn-on and facilitates lossless zero voltage switching (6.3b). Once the right leg transition is complete, the primary current freewheels through transistor Qa and the body diode of switch Qc. This shunts the body diode with the MOSFET Rds(on) switch resistance, thus lowering conduction losses. Qc can now be switched on

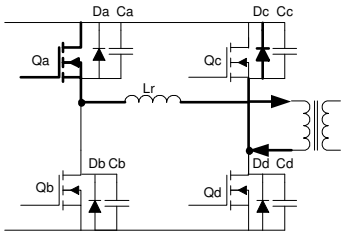
any time during this period (6.3c). Qa is then turned off and the primary current will now flow through the capacitance Ca charging it to the upper rail voltage. However, just the opposite happens to Qb, which previously had the full input voltage across its terminals; this begins the left leg transition. The resonant transition forces the voltage across Qb to zero, enabling lossless switching to occur (6.3d). Once switch Qb is turned on, the transformer primary is placed across the input supply rails and power will commence to transfer to the secondary, since switch Qc is already on (6.3e). Switch Qc is then turned off and the current continues to flow through the output capacitor, increasing the drain-to-source voltage from zero to the full input supply voltage. The output capacitance of the lower switch Cd is simultaneously discharged via primary current (6.3f) and, once the body diode conducts, Qd can be switched on. The power conversion interval is concluded with Qd and Qa switching having already been described.



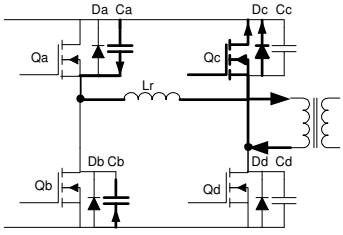
6.3(a)



6.3(b)



6.3(c)



6.3(d)

6.3(e) 6.3(f)

Fig. 6.3 ZVS Switching Mechanism

6.2 Phase Shifting Control

Phase shifting control is used to adjust the phase shift between the alternate switches in the right and left legs of the bridge, while switching at a constant frequency. The circuit configuration used to achieve this is shown in Fig. 6.4.

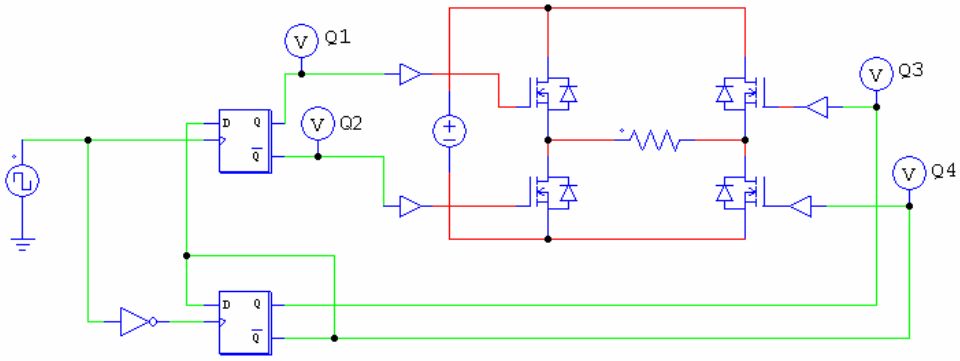


Fig. 6.4 Phase Shifting Logic

The circuit consists of two positive edge triggered D-type flip flops, with the positive edge of the clock pulse triggering the upper flip flop and the negative edge triggering the lower flip flop. The duty cycle of the input clock pulse is reflected between outputs Q1 and Q4 and between Q2 and Q3 which are connected to the diagonal MOSFETs. A simulation is done with an input clock signal

having a 20% duty cycle, as shown in Fig. 6.5. Both Q1 and Q4 outputs have a constant 50% duty cycle but phase shifted by 20%, the same applies for outputs Q2 and Q3. As a consequence of using flip flop logic, the output frequency is half the input clocking frequency. Hence, the MOSFETs are switched at half the clocking frequency of the D-type flip flops.

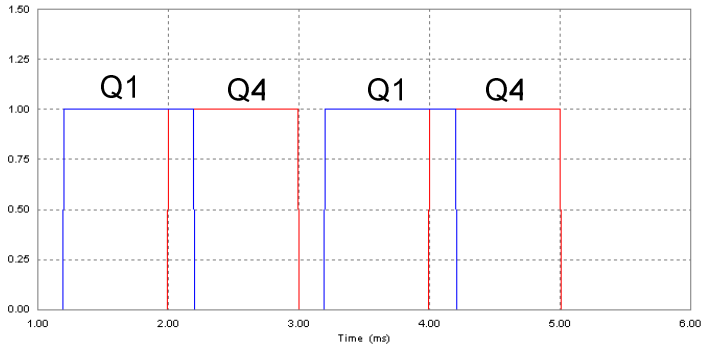


Fig. 6.5 Phase Shifting Logic Ouput

The phase shifting circuit is connected to the switching MOSFETs via gate drive transformers. The function of a gate drive transformer is to transmit the ground reference gate drive pulse across large potential differences to accommodate floating drive implementations. It handles low power but high peak currents to drive the gate of a power MOSFET. The gate drive transformer is driven with a constant amplitude signal. The gate drive transformers operate in both the first and third quadrant of the B-H plane. Fig. 6.6 shows one of the three converter modules interfaced to the GAL26CV12 control circuitry. With reference to flip flop A in Fig. 6.6, during the first clock cycle when Q is on, a positive voltage across the winding of the gate drive transformer is applied. This switches on the upper MOSFET in the left hand leg of the bridge circuit, while at the same time a reverse bias is applied to the bottom MOSFET preventing it from switching on. During the next clock cycle Q is off and the lower MOSFET switches on whilst the upper MOSFET is kept in the off state. The same cycle occurs for flip flop B. Since a transformer can only be magnetized in

one direction at a time, this prevents any parasitic turn on and cross conduction conditions from occurring.

The phase shifting circuit is implemented on a GAL26CV12 programmable logic device (PLD). The inputs to the GAL26V12 consist of three PWM signals generated from the TMS320F2812 DSP, with each signal having the appropriate switching pattern for the particular converter module circuit. The GAL26CV12 performs the phase shifting and drives the converter with a modulating duty cycle generated by the DSP.

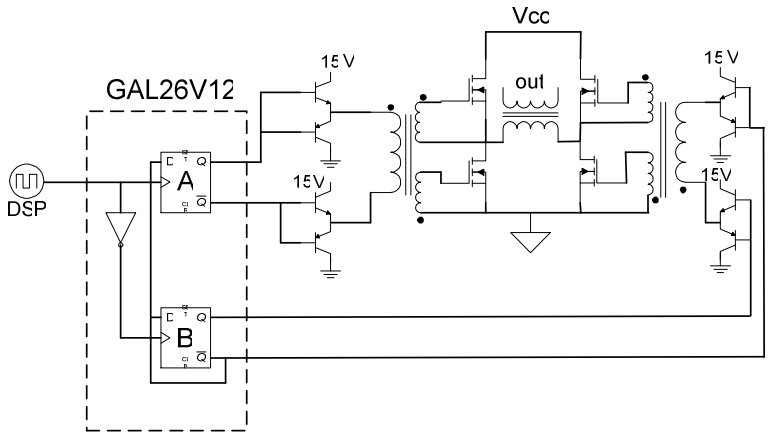


Fig. 6.6 Phase Shifting and Gate Driver Control

6.3 Digital Control Solution

The complete digital control solution is shown in Fig. 6.7 and consists of a combination of feedback and feedforward loops. The feedforward loop consists of the PLL with details of its purpose already discussed in chapter 4 section 4.2. The feedback loop has also been introduced in chapter 4 section 4.3 and a detailed analysis can be found in chapter 7.

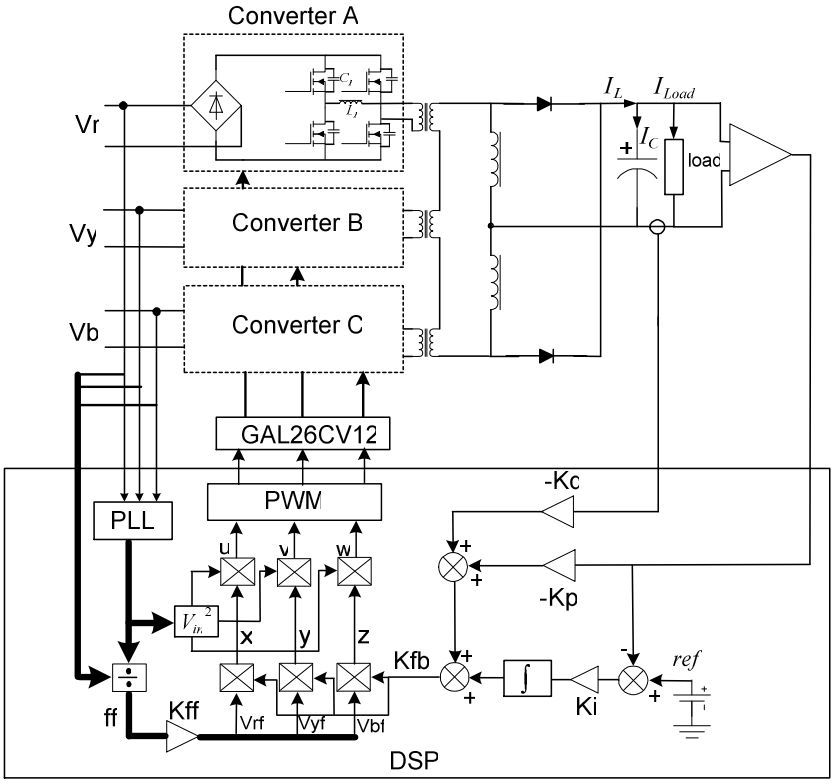


Fig. 6.7 Digital Control Implementation

The TMS320F2812 DSP algorithm is controlled by the on-chip timer T1, which generates a asymmetric ramp waveform internal to the DSP and provides the main time base for interrupt generation, PWM outputs and ADC conversions. After the ADC interrupt takes place an interrupt service routing is run, which reads the converted values from the ADC result registers. At the end of the control algorithm the PWM is updated with the required duty cycle value. This process is shown in Fig. 6.8 where a compare register is used to hold the duty cycle values shown as Ref A in Fig. 6.8. The value of the compare register is constantly being compared with the value of the timer counter. When the values match, a transition at the associated PWM output occurs. A second transition occurs when the timer period ends, in this way an output pulse is produced that is proportional to the value in the compare register. This process is repeated for each time period.

The ADC sampling takes place at 100kHz. The PWM is generated at 200kHz since running an asymmetric ramp produces two PWM outputs for every sampled input. However, the phase shifting GAL26CV12 logic results in a halving of the frequency, thus the rectifier is run at 100kHz.

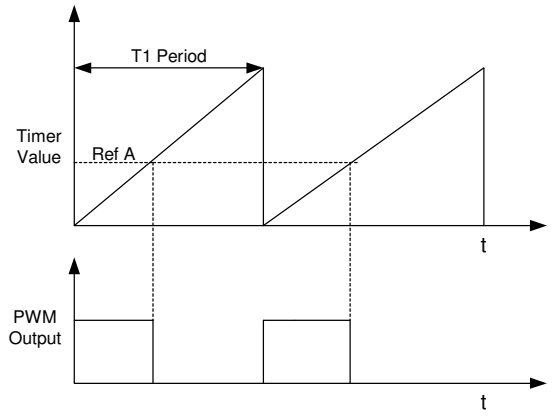


Fig. 6.8 PWM Generation

The process starts off by initialising all the required peripherals including the system clocks and sets up the ADC interrupts. The CPU then waits for the ADC interrupt event. When the interrupt takes place the ADC performs the required voltage samples which are then read by the CPU and loaded into the required result registers. The mains phase voltage samples are then fed into the PLL routine which generates three-phase sinusoidal voltage representations. The actual mains voltage signals (Vr,Vy,Vb) are divided by the PLL outputs resulting in three PU error signals. These PU error signals form the feedforward loop discussed in detail in chapter 7.1 and are used for the compensation of mains voltage deviations (see chapter 4.2). These PU error signals are scaled such that under nominal mains conditions the feedforward error signals represent 50% of the maximum PWM output (shown as ff in Fig. 6.7). These PU error signals are multiplied by the feedforward gain Kff, which would always have a value of unity so as not to distort the error ratio.

Therefore, if for example the mains phase voltage Vr were to drop by 50%, then the corresponding error signal Vrf would increase by 50% to the maximum PWM output. Likewise, if the mains phase voltage Vr were to increase to twice the nominal value then the Vr signal would drop to zero PWM output. These feedforward signals are multiplied and normalized with the feedback signal Kfb. The resultant x,y,z, signals are used to vary the gain of the driving V^2 signal, resulting in an independently controlled PWM outputs shown as u,v,w. These signals then feed the GAL26CV12 phase shifting logic. Once the PWM compare registers have been updated, the routine resets and acknowledges the interrupt, then proceeds and waits for the next ADC interrupt to take place. The software source code can be found in the attached CD, and a flow chart is shown in Fig. 6.9.

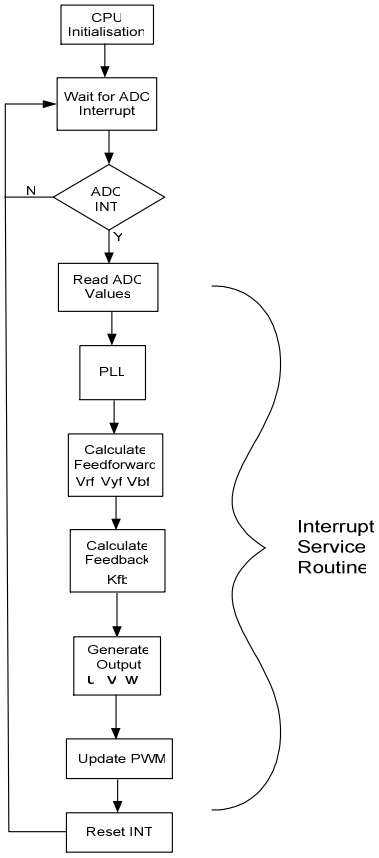


Fig. 6.9 Software Flowchart

6.4 Summary

The three-phase rectifier is controlled by a TMS320F2812 DSP with the software implementation been discussed and shown graphically by means of a program flow chart. The DSP runs on a continuous loop, triggered by the internal timer T1 which runs the ADC interrupt service routine and also provides the PWM timing. The digital control strategy has been described with the feedforward loop been able to compensate for mains phase imbalances ranging from ±50% of the nominal phase voltage. This approach enables the system to able to provide constant power flow during conditions of non-ideal mains, due to the ability to independently control each power converter module. This feature enables redundancy, in that if one phase were to be lost, power can still be transferred via the remaining converter modules. Having, as well, a feedback loop, the system is also able to provide output voltage regulation. The next chapter examines in detail the feedback loop structure.

6.5 REFERENCES

[1] Y. Chuang and Y. Ke, "A Novel High-Efficiency Battery Charger with a Buck Zero-Voltage-Switching Resonant Converter", IEEE Transactions on Energy Conversion, Vol. 22, No. 4, pp. 848-854, Dec. 2007.

[2] K. Lui and F.C. Lee, "Zero-Voltage Switching Technique in DC-DC Converters", IEEE Transactions on Power Electronics, Vol. 5, No. 3, pp. 293-304, July 1990.

[3] C. Wang, "A Novel Zero-Voltage-Switching PWM Boost Rectifier with High Power Factor and Low Conduction Loss", IEEE Transactions on Industrial Electronics, Vol. 52, No. 5, pp. 427-435, April 2005.

7 STABILITY ANALYSIS

In the examination of control systems, Phelan [1] recognised that the fundamental limitation on performance is the physical capability of the system. Since there is always a limit on the output level, the rate of response of the system should be considered in the design of any feedback control system. Phelan showed that of the three usual control computations, (proportional, integral, and derivative), only the integral is really effective in the forward loop. He claimed that the proportional and derivative actions are more effective in the feedback loops.

Using the control methodology introduced by Phelan, known as pseudo derivative feedback control (PDF), an analysis of the power converter prototype using this control is undertaken and a suitable system model is derived. From this model, further analyses are undertaken to determine the stability limits of the overall system.

7.1 Analysis of Control Systems

The PI or PID controller has been very popular in industry, because of its simple structure and relatively easy tuning procedures and acceptable performance [2]. A PI controller is generally good for eliminating long term errors, but is prone to overshoot, as it introduces a zero into the closed loop system. As the power converter prototype needs to have a high disturbance rejection capability, a simple PI controller is not sufficient and a more suitable control strategy needs to be implemented.

A PID controller will, in theory, provide a better disturbance rejection than a pure PI controller with the derivative term used for dampening oscillations. Classical PID control of a closed loop system can produce a satisfactory damping ratio and steady-state error, in response to a set point

input. However, it does not address issues such as risetime, bandwidth, robustness and system stiffness [3]. Therefore, a PID controller cannot be used in every case.

A PDF controller has the integral term, dedicated to the steady-state error, located in the forward path, while the remaining terms, dedicated to assigning the desired closed loop response (stability, responsiveness, disturbance rejection, etc.) are located in the feedback path. The PDF controller does not contribute to closed loop zeros, and hence it is not expected that the dynamic performance of the closed loop response will deteriorate [4]. PDF control is strongly robust and possesses good dynamic control performance [5]. The complete PDF control strategy used to control the converter prototype is shown in Fig. 7.1.

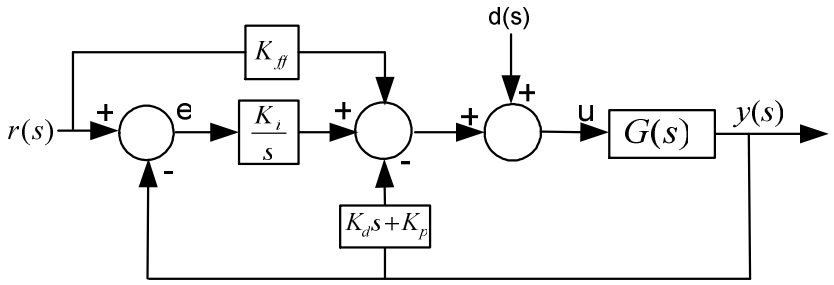


Fig. 7.1 Plant with PDF Controller

As shown in Fig. 7.1 the PDF controller consists of a main control loop, containing an integrator which assures there is no steady-state error in the system closed loop response. The feedback loops determine the dynamic response of the system. An additional feedforward loop with gain K_{ff} is introduced to provide compensation for any input variations as described in chapter 4 section 4.2. This feedforward loop injects the command ahead of the integral gain, making the system more responsive to input variations. In the case of the power converter prototype, this improvement in a response to input variations translates into an ability to deal with mains voltage imbalance. In Fig. 7.1 *r(s)* refers to the input voltage reference in the converter system, with

d(s) representing a disturbance which comes from a load step change. The converter PWM command signal is shown as u. The PDF controller is able to eliminate integral windup, which occurs when a system is commanded to deliver more than its capability, as well as the derivative kick, occurring as a result of rapid changes in the reference signal [5]. As the converter prototype is a buck derived converter, it can be modelled as a simple buck topology. The small signal equivalent circuit is shown in Fig. 7.2.

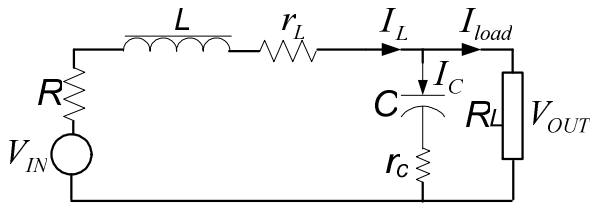


Fig. 7.2 Buck Equivalent Circuit Model

A typical buck converter includes an LC filter arrangement as shown in Fig. 7.2, with the list of symbols introduced.

V_{IN} = input voltage

V_{OUT} = output voltage

R = input impedance (impedance of input filter and combined MOSFET on-resistance)

L = inductor

C = output capacitor

r_L= DC resistance of inductor

r_C = equivalent series resistance of capacitor

R_L = load resistance

In general, the relationship between the time-varying current $I_L(t)$ passing through the inductor L and the time-varying voltage $v_L(t)$ across the inductor, is described by the following equation:

$$I_L(t) = \frac{1}{L}\int v_L(t)dt \tag{1}$$

The time-varying current through a capacitor $I_C(t)$ with capacitance C, connected to a time-varying voltage source $v(t)$, is related by the following equation:

$$I_C(t) = C\frac{dv_C(t)}{dt} \tag{2}$$

The load current I_L from Fig. 7.2 can be represented as follows:

$$\begin{aligned} I_{load} &= I_L - I_C \\ &= \frac{1}{L}\int v_L(t)dt - C\frac{dv_C(t)}{dt} \end{aligned} \tag{3}$$

Under dynamic conditions, such as a step load change, the load current changes rapidly according to the relationship shown in (3). Under a load change the derivative action of the capacitor has a large influence on the load current rather than the inductor which has a slower integral action. Accordingly, under dynamic conditions, the load current exhibits a derivative action. Hence, the current feedback has a derivative component without any additional differentiation needing to take place. This small signal buck equivalent circuit is used to derive the open loop transfer function, and with the addition of the PDF controller the closed loop transfer function is also derived, which allows for stability analysis to take place. The details are discussed in the next section.

7.2 Stability and System Modelling

The open loop transfer function of the buck equivalent circuit of Fig. 7.2, and represented as *G(s)* in Fig. 7.1, is derived as follows:

$$\frac{V_{out}}{V_{in}} = \frac{\dfrac{1}{(1/R_L) + \dfrac{1}{r_C + (1/sC)}}}{sL + (R + r_L) + \dfrac{1}{(1/R_L) + \dfrac{1}{r_C + (1/sC)}}}$$

$$= \frac{(CR_L r_c)s + R_L}{L(R_L C + r_C C)s^2 + [L + C(RR_L + r_L R_L + Rr_c + r_c r_L + R_L r_C)] + (R_L + R + r_L)} \qquad (4)$$

When $R_L >> r_L$, r_C and R, equation (4) can be simplified to

$$\frac{V_{out}}{V_{in}} = \frac{r_C Cs + 1}{LCs^2 + [(L/R_L + C(R + r_L + r_C)]s + 1} \qquad (5)$$

Equation 5 represents the open loop transfer function of the buck equivalent circuit model. From measurements of the power converter prototype the following equivalent circuit component values were found; C=4.1mF, r_C=1.8mΩ, R=850mΩ, L=38μH, r_L=85mΩ and R_L=5Ω. Substituting these values into (5) gives:

$$G(s) = \frac{7.38\times10^{-3}s + 1}{0.15\times10^{-6}s^2 + 2.6\times10^{-3}s + 1} \qquad (6)$$

Equation 6 can be rewritten as

$$G(s) = \frac{As + 1}{Bs^2 + Cs + 1}$$

The closed loop transfer function for Fig. 7.1 is determined using Mason's Gain Rule which is stated as follows:

$T = \frac{\sum_k P_k \Delta_k}{\Delta}$ where,

T = transfer function

k = number of forward paths

P_k = the kth forward path gain

Δ = 1-∑loop gains + ∑nontouching loop gains taken two at a time - ∑nontouching loop gains taken three at a time + ∑nontouching loop gains taken four as a time - …

Δ_k = Δ - ∑the loop gain terms that touch the kth forward path.

By applying Mason's Gain Rule to Fig. 7.1 the following was found:

Since there are two paths from r(s) to y(s)

$P_1 = K_{ff}$ G(s) and $P_2 = \frac{K_i}{s}$ G(s)

There are two loops

$L_1 = -\frac{K_i}{s} G(s)$

$L_2 = -G(s)\left(K_d s + K_p\right)$

There are no loops that are nontouching therefore

$\Delta = 1-(L_1+L_2)$

To find Δ_1 the loops touching path P_1 are removed from Δ hence $\Delta_1=1$. Similarly $\Delta_2=1$.

Mason's technique now yields:

$$T = \frac{P_1\Delta_1 + P_2\Delta_2}{1-(L_1+L_2)} \tag{7}$$

After substituting and expanding (7), the closed loop transfer function becomes

$$\frac{y(s)}{r(s)} = \frac{AK_{ff}s^2 + (AK_i + K_{ff})s + K_i}{(B+K_dA)s^3 + (C+K_p+K_d)s^2 + (K_p+1+AK_i)s + K_i} \tag{8}$$

From (8) the gain K_{ff} in the numerator is the feedforward gain and is expected to have a value of unity. As a result the term AK_{ff} is significantly smaller than $(AK_i + K_{ff})$, since A=7.38x10^{-3}, and the s^2 term can be omitted from the numerator. In the denominator the s^3 term can be omitted since K_d is multiplied by A, therefore the resultant coefficient of s^3 is approximately 1000 times smaller the s^2 coefficient. Hence, these second and third order terms can be omitted and the transfer function simplified to

$$\frac{y(s)}{r(s)} = \frac{(AK_i + K_{ff})s + K_i}{(C+K_p+K_d)s^2 + (K_p+1+AK_i)s + K_i} \tag{9}$$

The transfer function from the disturbance input to output is determined by setting r(s)=0 in Fig. 7.1. The transfer function can be written as

$$y(s) = \frac{G_1(s)}{1+\frac{K_i}{s}G_1(s)}d(s) \tag{10}$$

Where $G_1(s) = \frac{G(s)}{1+(K_ds+K_p)G(s)}$ (11)

Substituting (11) into (10) and rearranging

$$\frac{y(s)}{d(s)} = \frac{As+1}{(B+K_dA)s^3 + (C+K_pA+K_d)s^2 + (K_p+K_iA+1)s + K_i} \tag{12}$$

In the denominator the s^3 term can be omitted since K_d is multiplied by A, therefore the resultant coefficient of s^3 is approximately 1000 times smaller the s^2 coefficient. Equation 12 can therefore be simplified to

$$\frac{y(s)}{d(s)} = \frac{As+1}{(C+K_p+K_d)s^2 + (K_p+AK_i+1)s + K_i} \tag{13}$$

From (13) it can be seen that the system is independent of K_{ff} and it can be concluded that the disturbance rejection characteristic is not affected by the feedforward zeros but is purely dependent on the closed loop zeros.

To ensure that there is no startup overshoot for the closed loop system; all the roots of the denominator in (9) should be real, therefore

$$\Delta = (K_p+1+AK_i)^2 - 4(C+K_p+K_d)K_i \geq 0 \text{ with } A=7.38\text{x}10^{-3} \text{ and } C=2.6\text{x}10^{-3} \tag{14}$$

As the gains, that are multiplied by A and C, result in very small values that do not contribute significantly to the system performance, they can be omitted and (14) simplifies to

$$(K_p+1)^2 - 4(K_p+K_d)K_i \geq 0$$

From which the following relationship can be obtained

$$K_i \leq \frac{(K_p+1)^2}{4(K_p+K_d)} \tag{15}$$

In order to obtain a system response with no startup overshoot, the system should be tuned using the constraints as shown in (15). Fig. 7.3 shows the simulated output voltage response Vout of Fig. 7.1 during a startup, with the gain variables of K_p=40, K_i=9 and K_d=3, which satisfies the requirements of (15). The values were chosen that give a realistic representation of a control system having the highest gain the proportional, followed by the integral and the differential having the lowest gain as is the common outcome from a tuned system. K_{ff} was set to 1 as discussed in chapter 6.3.

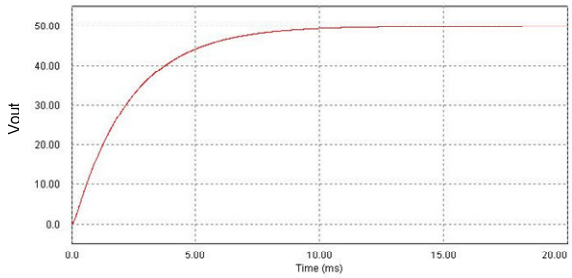


Fig. 7.3 System without Startup Overshoot

The simulation is once again performed with the gain values of K_p=40, K_i=11 and K_d=3 thereby not complying with the requirements of (15). The startup response is seen in Fig. 7.4.

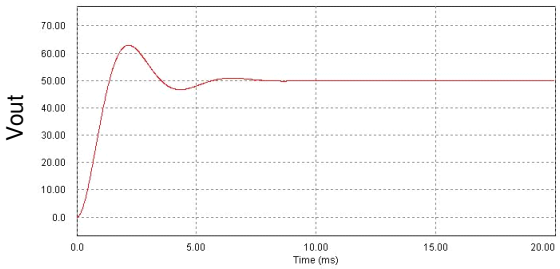


Fig. 7.4 System with Startup Overshoot

This shows the need for careful selection of the various gain values in order for the system to have the desired response. The Bode magnitude and phase plots of the loop response are shown in Fig. 7.5, with the restrictions imposed by (15). Having the same gain values of K_p=40, K_i=9 and K_d=3.

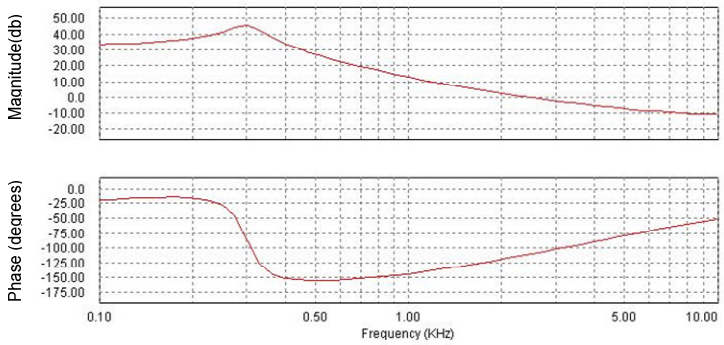


Fig. 7.5 PDF Control Loop Response

The system exhibits a bandwidth of approximately 2.5kHz with a maximum phase shift of -155°, indicating a high degree of stability, since the maximum phase shift is relatively far from -180°, which is the point at which the system would become unstable. In order to see what influence each component of the characteristic equation, namely the proportional, integral and differential has on the overall stability of the system, each of them were individually increased and the Bode response observed. Firstly, the integral component has its gain increased from 9 to 20 with the corresponding Bode plot shown in Fig. 7.6.

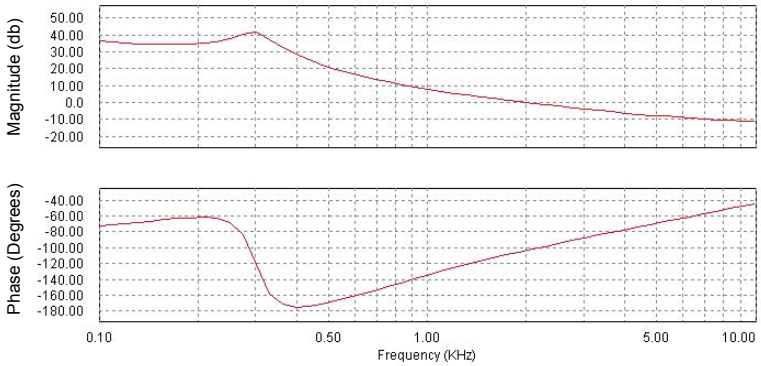


Fig. 7.6 PDF Control with High Integral Gain

From Fig. 7.6 it can be seen that the bandwidth remains unchanged at approximately 2.5kHz, while the maximum phase shift has increased to -167° at 24db. Hence, large integral gains will tend to drive the system towards instability since a phase lag is effectively introduced into the system. Higher integral gain values will cause the phase shift to cross the -180° stability boundary with the magnitude greater than 0db. The proportional gain was increased to 100, with the Bode responses shown in Fig. 7.7.

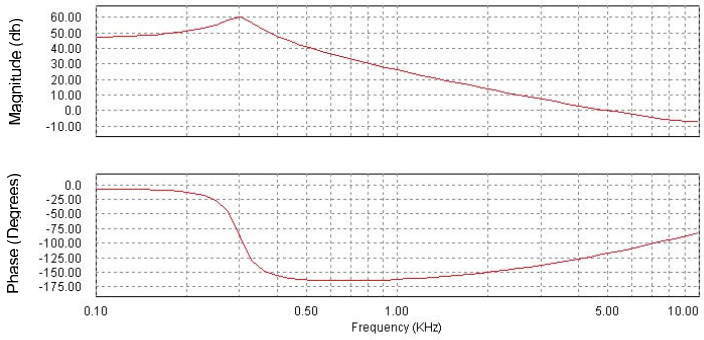


Fig. 7.7 PDF Control with High Proportional Gain

The Bode magnitude and phase plots reveal that the bandwidth has increased to 4.6kHz, while the maximum phase shift has increased to -161° at 26db. Hence, an increase in the proportional gain has

the advantage in that the system bandwidth also increases, but eventually the system will tend to produce instability under transient conditions due to the phase shift coming within close proximity of -180°.

The differential gain K_d was increased from 3 to 6 with the corresponding Bode plots (Fig. 7.8) showing the bandwidth had increased from 2.5kHz to 4kHz, while the maximum phase shift had decreased from -155° to -128°.

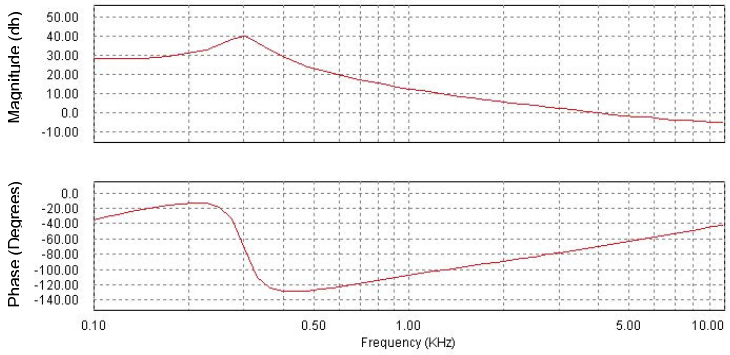


Fig. 7.8 PDF Control with High Differential Gain

Upon further increasing the differential gain value to 11, resulted in a phase shift of approximately -175°, from 400Hz up to 2.5kHz, after which the phase shift begins to decrease, the system therefore has an area of instability. This shows that although an increase in the differential gain will make the closed loop system more responsive, larger values of differential gain will result in poor phase margin (Fig. 7.9). Practically it is accepted that the minimum phase margin should be 45º.

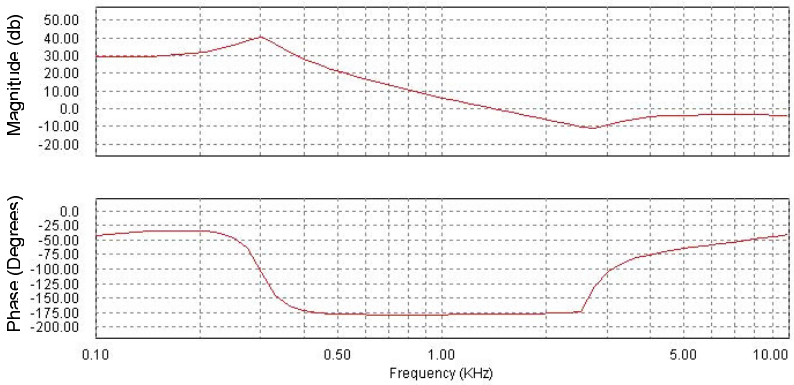


Fig. 7.9 System Instability with High Differential Gain

The numerator of the closed loop transfer function was examined to determine the location of the zero and the effect this will have on the system performance. The zeros of a response affect the amplitude of a response but not the nature of the response, that is, exponential, damped sinusoid, and so on. The location of the zero is found from examining the numerator of (10) and shown in (16).

$$s = \frac{-K_i}{(K_{ff} + AK_i)} \text{ with } A=7.38\text{x}10^{-3} \qquad (16)$$

Selecting the integral gain value already used K_i=9, and with the feedforward gain K_{ff} set to unity equation 13 was solved. The zero was located at -8.4 on the real axis of the s-plane, while the respective roots, found by solving the characteristic equation of (10) are located at -0.6 and -0.3. Since the zero is located far away from the roots its effect can be ignored and the system can be modelled as a two pole system.

7.3 Discrete System Analysis

Since the system is digitally controlled it makes sense to conduct an analysis into how this affects the overall performance of the converter. Firstly, the effects of delays are investigated; The following considerations are based on the analysis of the time delays that are associated with the regulating the output voltage under DSP control.

The switching frequency of $f = \frac{1}{T} = 100kHz$ is selected. The TMS320F2812 DSP has a 12.5Msamples/s 12 bit analog-to-digital converter, and as such conversion delay can be neglected. The effect of the time delay from the instant the DSP PWM signal goes high until the respective converter switch also goes high was found to be 0.7μs. This can be represented by the function e^{-sT}.

The switching delay is represented by $G_{sw} = e^{-s0.07T}$ (16)

Due to the calculation of the control commands required to produce the correct output voltage, a delay of one full pulse period occurs [6].

$G_{calc} \approx e^{-sT}$ (17)

Additionally, the sample and hold function of the PWM causes a half period delay [6].

$G_{pwm} = e^{-sT/2}$ (18)

Which is valid if the PWM is updated only once per pulse period. For a double update mode, the delay time introduced by the PWM operation is reduced to a quarter pulse period [7]. The total delay transfer function of the DSP is

$G_{del}=G_{calc}xG_{sw}xG_{pwm}$

$$= e^{-sT} e^{-s0.07T} e^{-sT/4}$$

$$\approx e^{-s1.25T} \qquad (19)$$

The system is now simulated using the values of K_p=40, K_i=9 and K_d=3 as in section 7.2 but with the delay transfer function (19) included. The simulation results are shown in Fig. 7.12.

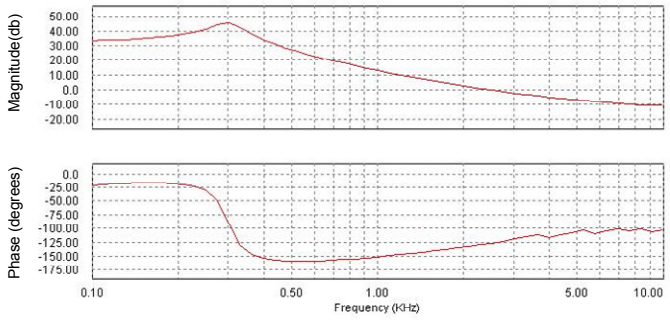


Fig. 7.12 System Response with Delay

The bode magnitude and phase plots reveal that the introduction of delay in the simulation results in a maximum phase shift of -158º. This is a 3º increase in phase shift from the simulation in Fig. 7.5 which had no delay component. The bandwidth is unchanged at 2.5kHz. Considering the 1.6 sample time delay in the converter prototype it was determined by simulation that the switching frequency at which the phase shift reaches -180º was 15kHz. The converter would have to switch at a frequency higher than 15kHz in order to have good phase margin.

In order to test the accuracy of the simulation model compared with the actual power converter system, a startup test is performed with values of K_p=40, K_i=9 and K_d=3. The system is first simulated with the mentioned gain values and having a reference voltage of 10V. Fig. 7.13 shows the response with the output voltage Vout reaching the setpoint after approximately 12ms.

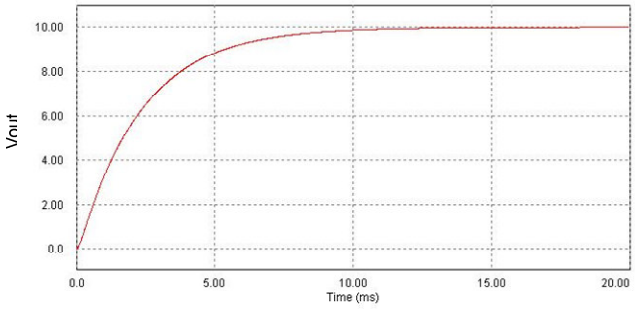


Fig. 7.13 Simulated Startup Response

The same gain values are applied to the power converter system with the startup response shown in Fig. 7.14.

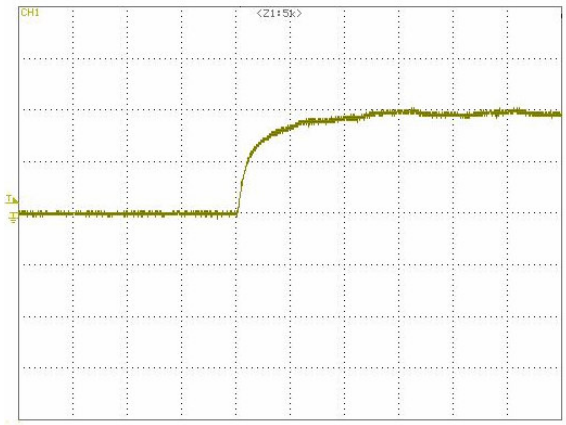


Fig. 7.14 System Startup Response (voltage scale: 5V/div, time scale: 5ms/div)

It can be seen that the system reaches the setpoint in 12-15ms and therefore shows that the simulated model is an accurate representation of the actual system. This is due to the high frequency sampling which reduces the delay times and results in the power converter system being able to be accurately modelled.

7.4 Conclusion

A complete s-domain control model has been derived, with the modelling of the prototype converter as a simple buck circuit having a PDF control loop. The closed loop transfer function has been derived and the system analysed. From the analysis it was shown that using the PDF control loop resulted in a system that is stable, as long as the control loop gain values remain within the acceptable limits. In order for the system response to be optimised, the gain parameters need to be tuned according to (12). Using a PDF controller has the advantage of no integral windup or derivative kick phenomenon which plagues conventional type controllers. From the analysis of the derived model, it was shown that using the PDF feedback control scheme resulted in an inherently stable power converter system. The analysis of the digitised system showed that processing delays reduce the phase margin, however high frequency sampling reduces the delays and results in the system behaving more like a time continuous system than a discrete system, making the modelling less complex. The experimental results presented in the next chapter will provide a more accurate understanding of the power converter prototype overall performance.

7.5 REFERENCES

[1] R.M. Phelan "Automatic Control System", Cornell University Press, Ithaca, N.Y. 1977.

[2] G.F. Franklin, "Digital Control of Dynamic Systems", 2nd Ed., Addison-Wesley, 1990.

[3] J. C. Hung, "Practical Industrial Control Techniques", International Conference on Industrial Electronics, Control and Instrumentation, Vol. 1, pp. 7-14, Sept. 1994.

[4] P. Paraskevopoulos, G. Pasgainos and K. Arvanitis, "New Tuning and Identification Methods for Unstable First Order Plus Dead-Time Processes Based on Pseudoderivative Feedback Control", IEEE Transactions on Control Systems Technology, Vol. 12, No. 3, pp. 455-464, May 2004.

[5] M. Tang and L. Chen, "The System Bandwidth Analysis in Electro Hydraulic Servo System with PDF Control", 5th Asian Control Conference, Vol. 3, pp. 1737-1745, July 2004.

[6] T. Nussbaumer, M.L. Heldwein, G. Gong, S. Round, and J. Kolar, "Comparison of Prediction Techniques to Compensate Time Delays Caused by Digital Control of a Three-Phase Buck-Type PWM Rectifier System", IEEE Transactions on Industrial Electronics, Vol. 55, No. 2, pp. 791-799, Feb. 2008.

[7] V.Blasko, V. Kaura and W. Niewiadomski, "Sampling of Discontinuous Voltage and Current Signals in Electric Drives: A System Approach", IEEE Transactions on Industrial Applications, Vol. 34, No. 5, pp. 1123-1130, Oct. 1998.

8 RESULTS

A three-phase 500W rectifier prototype, using three single-phase full bridge modules, each connected to a phase voltage in a star connected system was constructed. The three modules have their output transformers connected together in series, feeding into a current doubler topology. The rectifier prototype is able to run up to full load under open loop control, however due to bandwidth limitations of the DSP the closed loop tests are performed at a reduced power level. This is because running the additional code performing the PDF control, involves slowing the DSP's operating frequency to 100kHz in order to prevent interrupt overrun. This in turn results in a lower PWM switching frequency, which saturates the output transformers at a voltage less than the 220Vrms mains voltage. This can be mitigated by recoding individual routines in assembler until the DSP is sufficiently able to be run at a frequency of 150kHz, which would allow mains voltages to be applied. In this chapter various tests are carried out on the converter with the results detailed and compliance issues discussed.

8.1 System Overview

The rectifier prototype (see schematic in appendix A) is controlled by a TMS320F2812 DSP which produces the required V_{in}^2 PWM switching pattern. This is achieved by feeding the mains input voltages through three stepdown transformers which step the voltages down from 220V to 25V. These transformers in turn feed three potentiometers used for adjusting the voltages, which in turn are fed into three differential amplifiers used to bring the voltages into the DSP input interface board (see attached CD). The input interface board, level shifts the voltages to the appropriate levels for the ADC ports on the DSP. In Fig. 8.1 a schematic of the system setup is shown.

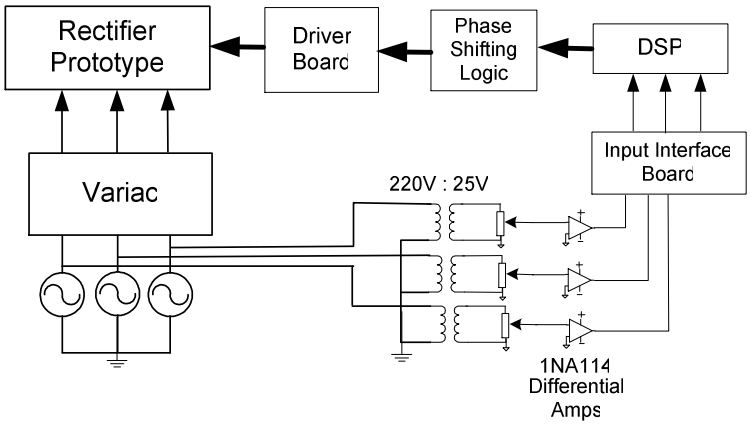


Fig. 8.1 System Overview

The input interface board brings in the mains voltages into the DSP at the correctly scaled values, where they are sampled and processed in order to provide the inputs for the digital PLL. The PLL provides the synchronisation such that the output Vin^2 waveforms generated by the PWM ports are synchronised with the mains voltages. Fig. 8.2 shows one of the mains phase voltages together with the DSP modulating V_{in}^2 output waveform in synchronism.

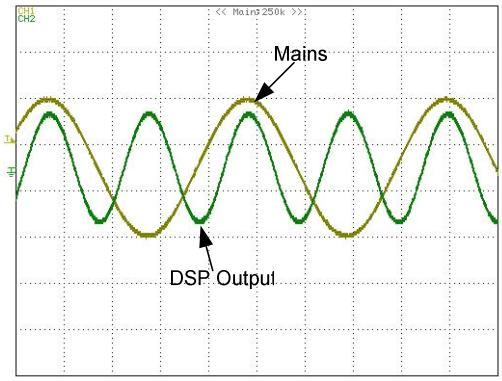


Fig. 8.2 DSP Synchronised with Mains

(voltage scale: Mains 20V/div, DSP 1V/div, time scale: 5ms/div)

The three PWM output waveforms from the DSP each get fed into a GAL26CV12 phase shifting IC. The phase shifting logic transforms the PWM signal into four output signals (two being complements), having a phase shift corresponding to the PWM duty cycle. Fig. 8.3 shows the DSP output PWM with a 50% duty cycle, and the corresponding GAL IC producing a 50% phase shifted output.

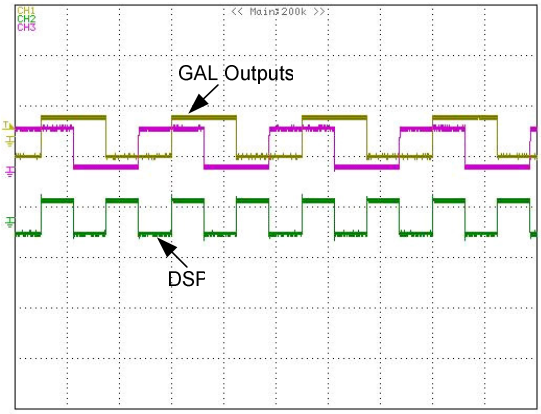


Fig. 8.3 DSP Phase Shifting (voltage scale: 5V/div, time scale: 5μs/div)

The signals from the phase shifting logic are transferred to the driver board which performs the necessary level shifting (5Vto 15V) and the switching of the MOSFET gate drive transformers (Fig. 8.1). These allow each rectifier module to be driven with the appropriate switching strategy. In Fig. 8.4 a DSP PWM output is shown with an 80% duty cycle. The diagonal MOSFET gate driver signals have the same duty cycle, as well as the output transformer primary, thus showing the correct and expected operation of the phase shifting control.

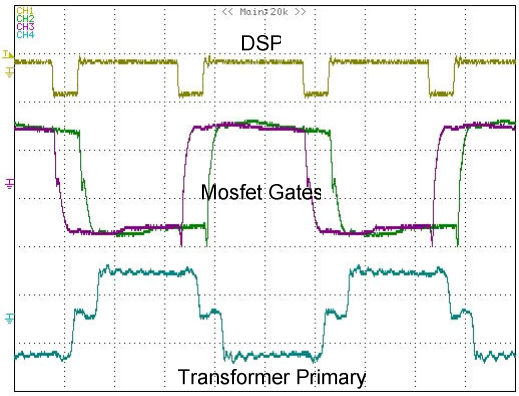


Fig. 8.4 Waveforms with 80% Duty Cycle

(voltage scale: DSP 5V/div, Mosfet 10V/div, Transformer 10V/div, time scale: 2μs/div)

The output transformers are connected in series in order to apply the summing function required. The waveforms of the three transformer primaries are shown in Fig. 8.5, with each having the V_{in}^2 switching pattern applied. Refer to chapter 6.1 for discussions on the topology details.

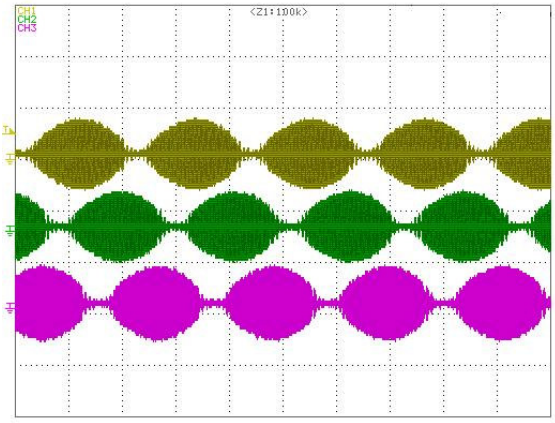


Fig. 8.5 Transformer Primary Waveforms (voltage scale: 20V/div, time scale: 5ms/div)

Finally, the variac (Fig. 8.1) is used to control the input voltage into the system since switching takes place at 100kHz and the minimum frequency in order for mains voltages (220Vrms) to be applied without transformer saturation is 150Hz. The calculation of transformer saturation limits are shown as follows:

$$\Delta B = \frac{vt}{2NA_e} \tag{1}$$

Where vt=applied volt seconds

N=number of primary turns=17turns

A_e=core cross-sectional area for ETD49=211x10^{-6}m

ΔB=twice the peak flux swing=300mT

v=phase voltage=325V

Equation (1) can now be rearranged

$$t = \frac{2\Delta BNA_e}{v} \tag{2}$$

$$= \frac{2 \bullet 0.3 \bullet 17 \bullet 211x10^{-6}}{325}$$

=6.6μs

This translated to a minimum frequency of 150kHz for mains voltage to be applied to the transformer without saturation taking place.

8.2 Zero Voltage Switching

The rectifier prototype is designed to use a ZVS strategy in order to eliminate MOSFET switching losses and so obtain maximum efficiency [1-2]. The MOSFET gate and drain source voltages (Vds and Vg respectively) are captured at the onset of ZVS, as shown in Fig. 8.6. The point at which the MOSFET starts to turn on is when the gate threshold voltage is reached; this is the point at which the MOSFET is able to carry current (Vth in Fig. 8.6). This point coincides with the conduction of the MOSFET body diode Vd, indicating that the drain source capacitance has been discharged clamping the device to zero volts, and can now be switched on. The rectifier is operated with a 3Ω load and approximately 40Vrms applied to the input. If more power were to be transferred to the load, the gate voltage would not exhibit the miller effect at Vth seen in Fig. 8.6 as a result of the miller capacitance. Under full ZVS operation the miller effect disappears.

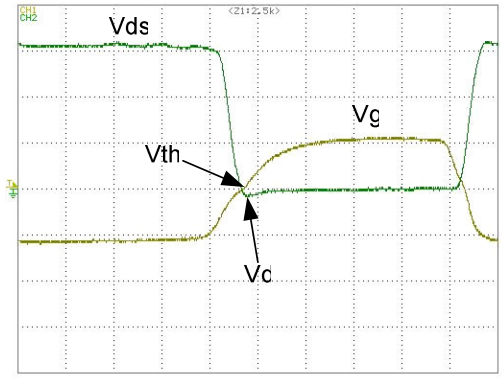


Fig. 8.6 Zero Voltage Switching (voltage scale: 10V/div, time scale: 500ns/div)

The transition point from hard switching to ZVS occurs with a line current of only 0.21Arms, which translates to approximately 11% of the full load current. ZVS operation requires circulating current to discharge the drain source capacitance, hence this is usually guaranteed under heavy load conditions, but under light loads there may not be enough circulating current to discharge the

drain source capacitance in time for the switching transitions resulting in hard switching taking place. ZVS operation takes place at approximately 11% of the full load due to the unique nature of the topology, with Fig. 8.7 showing a schematic of the principle in operation.

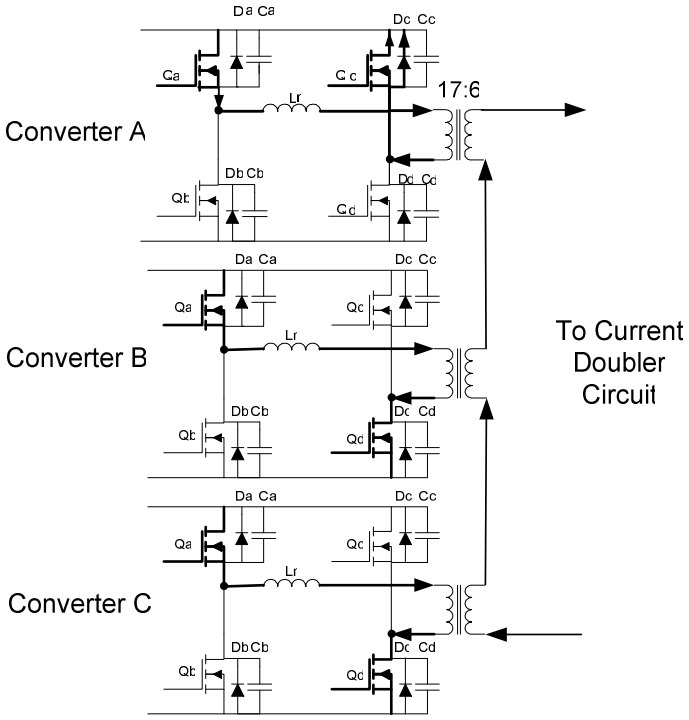


Fig. 8.7 Topology Schematic

Each bridge circuit has two switching states, one being the ON state when the diagonal MOSFETS are turned on and power is transferred to the output circuit via the transformers. Converter B and C are shown in this state in Fig. 8.7. The other state is the OFF state when both corresponding MOSFETS are on shorting the transformer primary (converter A). When this OFF state takes place, since the three transformer secondary windings are connected in series together, additional circulating current is reflected into converter A through the transformer turns ratio from the other two converters operating in the ON state. This adds to the resonant current already present in the converter module in the OFF state, thereby contributing additional current for the ZVS operation.

As a result ZVS operation can occur at light loads which has the added benefit in that high efficiency operation can be maintained during operation even while running at reduced loads.

8.3 Startup Response

The startup response of the rectifier prototype employing a conventional PI controller and a PDF controller is analysed. In order compare the responses of the two controller types, the PI controller has its gain values adjusted in order to give a single overshoot, which translates to a damping factor of around 0.7 for a second order system, thus ensuring the system is not overdamped. The values for the integral and proportional gains that provided the required output response were found to be K_i=50 and K_p=20 respectively. These gain values are applied to both the PI and the PDF controller. In addition, the current loop, which forms the derivative part of the PDF control, has a gain value selected that is small enough not to introduce instability into the system; the details have already been discussed in chapter 7 section 7.2. A gain value of 10 was chosen for this purpose. The startup output voltage of the power rectifier prototype using both the PI and the PDF controller is shown in Fig. 8.8.

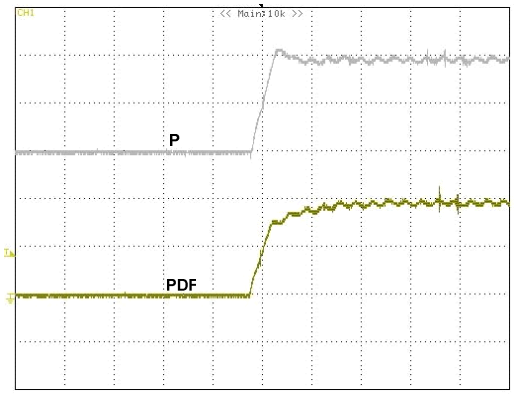


Fig. 8.8 PI and PDF Startup Response (voltage scale: 10V/div, time scale: 10ms/div)

As can be seen from Fig. 8.8, the system under PI control exhibits overshoot during the startup before settling, this takes approximately 12ms. Under PDF control no overshoot takes place, and the settling point is reached after approximately 27ms. Thus, the system under PI control has a faster rise time compared with the PDF controller; however this results in overshoot taking place. Although a PI controller can be critically damped resulting in no overshoot, this requires careful tuning, whereas the PDF controller will naturally ramp up to the setpoint, since the proportional component of the loop is subtracted from both the integral and current component, thus reducing the output voltage as it approaches the setpoint. This is confirmed by simulation as shown in chapter 4 section 4.3. The rise time of the output voltage can be adjusted by changing the proportional gain, for example if the rise time needed to be reduced then the amount of proportional gain needs to be reduced. Fig. 8.9 shows the startup output voltage under PDF control, one with a proportional gain of 20 the other with a gain of 40 and both with the same integral and current gains.

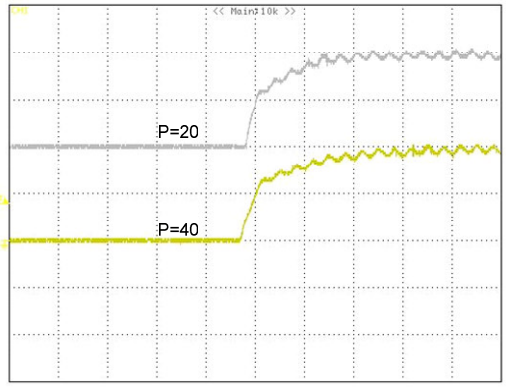


Fig. 8.9 PDF Startup Responses (voltage scale: 10V/div, time scale: 10ms/div)

From Fig. 8.9 one can see that as the proportional gain is increased the rise time also increases, in this case it takes approximately 38ms to reach its setpoint having a proportional gain of 40. The response is however quicker with the smaller proportional gain, resulting in approximately 27ms rise

time. This is a useful feature of the PDF control, as it means that a system is able to achieve a exponential ramp response naturally, without incorporating complex control strategies, thus saving DSP memory and or the need for additional circuitry, thus providing a cost saving benefit.

8.4 Load Step Response

The load step response is tested by applying the same PI and PDF control loops having the same gains as already described in 8.3. The system is made to undergo a load step change from 2Ω to 20Ω with the output power at 150W at 2Ω. The output voltage during the load step change is shown in Fig. 8.10.

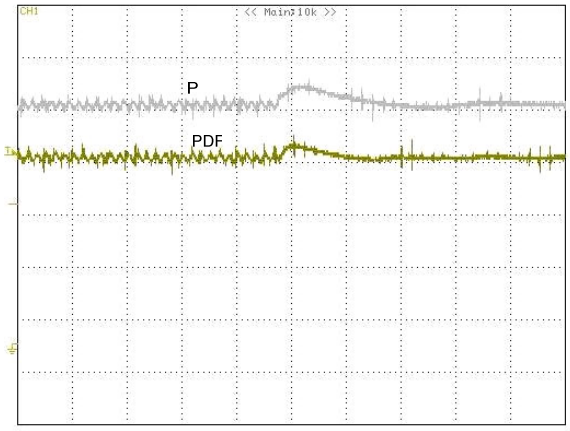


Fig. 8.10 Output Voltage Under Load Step (voltage scale: 5V/div, time scale: 20ms/div)

The output voltage under PI control produces a 12.5% overshoot and has a settling time of approximately 70ms, while under PDF control the system produces 8% overshoot with a settling time of approximately 40ms. Therefore, it is shown that the PDF control produces an improved response under a load step change. However, since digital signal processors always result in time delays, mainly due to the following three reasons:

1) sampling of continuous current and voltage quantities [3];

2) calculation time of the DSP[4];

3) PWM Generation [5].

Each of these time delays introduces a phase shift in the control loop, which reduces, in total, the achievable bandwidth or diminishes the closed loop system stability [6] (Chapter 7.4). The following methods are required to provide a further improvement in the load step response of the system.

1) Higher sampling rates reducing the delays.

2) Optimisation of the PDF control through tuning.

3) Compensation.

The higher sampling rates result in increased processing and thus reduce the delays in the DSP. Also, by correctly tuning the various gain values used in the control loop the response can be optimised. This can be achieved using the various traditional methods such as the Ziegler-Nichols or Cohen-Coon.

Another method to improve performance is to add compensation, which provides an increased bandwidth while still maintaining stability. Compensation methods recommended for buck derived converters are discussed in [7-9]. A variety of lead type compensators are discussed that could be used to provide an improved performance. These include a type 1, type 2 and type 3 controllers. Type 1 is simplistic and has poor transient response, it is recommended to use type 2 or type 3, with type 3 giving the best phase margin and transient response.

8.5 IEC1000-3-2 Compliance

The current THD is an important indicator of the level of distortion the waveform has and can be used to determine whether the product meets the IEC1000-3-2 standard, which is a requirement for telecommunication power converters. The limits of harmonics for each phase of the line current are shown in table 1 in the introduction chapter. These limits are absolute and therefore not related to the power ratings of the equipment. The limits are applicable to steady-state harmonic currents only. The line current THD for one phase of the rectifier prototype was analysed and the trend line shown in Fig. 8.11. The other phases showed similar results.

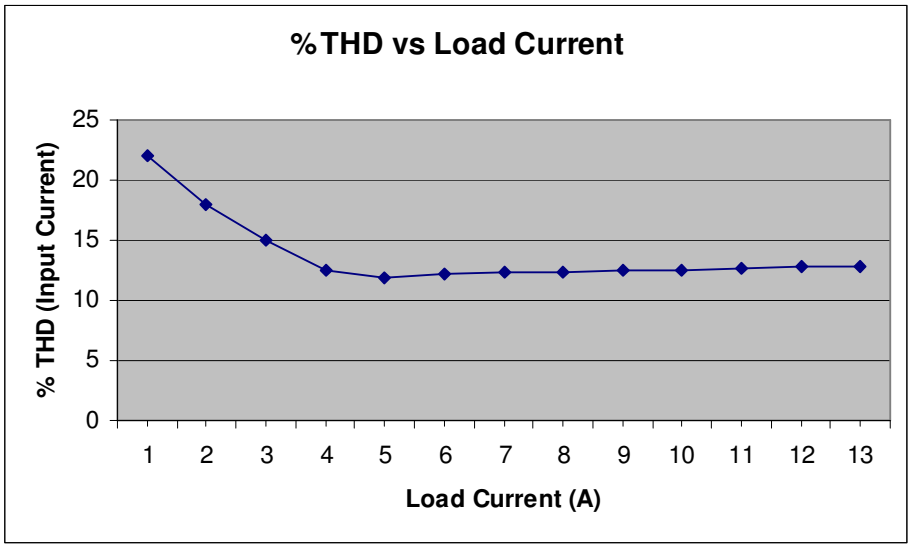


Fig. 8.11 Percentage THD vs Load Current

As seen from Fig. 8.11, there is a clear trend of a decreasing THD up to 5A of load current, which corresponds to a minimum THD of 11.9%. The THD remains relatively constant up till full load (13A). The line current harmonics are shown in Fig. 8.12.

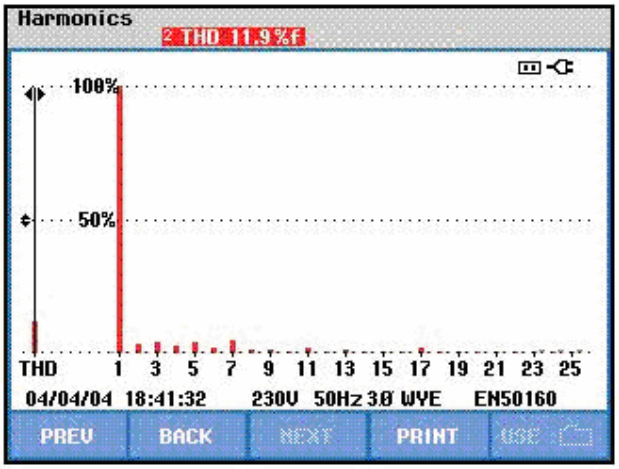


Fig. 8.12 Line Current Harmonics

A calculation of the THD is performed by using the input current rms values in the following equation:

$$\%THD = \frac{\sqrt{\sum_{n=2}^{40} I_n^{\,2}}}{I_F} \times 100 \qquad (1)$$

Applying the current harmonic magnitudes as dictated by the IEC1000-3-2 regulation to (1), having the input fundamental current component I_F at 2A, as this is the maximum expected input current for the rectifier prototype. The required percentage THD in order to comply with the IEC1000-3-2 standard is calculated to be 153%. The THD values shown in Fig. 8.11 are well below the actual required values. Having an input fundamental current component I_F of 26A will result in a THD of 11.7% being required to comply with the IEC1000-3-2 standard. Thus, the prototype can only be used at power levels below 6.5kW. The current THD can however be further reduced. This can be achieved by the use of a three-phase dynamic feedforward loop which would be used to balance the power drawn by the individual three power converter modules.

A control method of balancing three-phase power using topologies comprising of three single-phase rectifier units is discussed in [10]. The control strategy is based on a current mode control that makes each DC-DC converter module have an output characteristic of a current source with a controlled voltage. This approach is implemented through two control loops. A current control loop (inner loop), which monitors the transformer primary information, creates the voltage-controlled current source. The second loop is a voltage loop (outer loop), which monitors the converter's output voltage and constantly programs the controlled current source to regulate the output voltage at a given set point. A THD of less than 5% has been documented using this control method. This method will transform the feedforward loop from regulating the power drawn between the converter modules by means of voltage balancing to a current balancing approach. Another approach is to connect the modules in a delta configuration thus reducing the triplen harmonics occurring in the neutral.

The displacement power factor between the phase voltage and phase current is 0.99, which is close to the unity power factor that is predicted by theory. However, as the IEC1000-3-2 standard that the prototype is tested against is independent of displacement power factor, and only related to the current harmonic component values, as dictated by the class A harmonic current limits (see chapter 1 section 1.1.2), the displacement power factor doesn't in any way influence the testing of the prototype against the IEC1000-3-2 standard. Fig. 8.13 shows the phase voltage and current drawn from the supply at a load of 5A and a load of 3Ω. The current THD ranged from 11.9% to 12.1% from 5A through to full load. The displacement power factor displayed a constant 0.99 over the range of the range of load current from 1A to 13A.

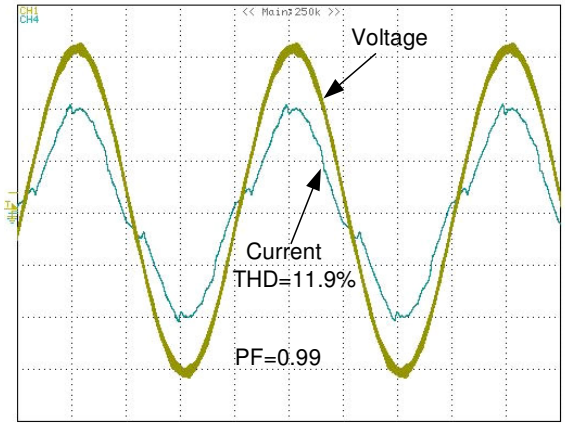


Fig. 8.13 Phase Voltage and Current Waveforms (voltage scale: 40V/div, current scale: 0.5A/div, time scale: 5ms/div)

8.6 Output Voltage Ripple

The prototype is tested under balanced three phase input voltages and a constant 3Ω load. The variac is used to incrementally increase the applied voltage and also the power transferred to the load. The output voltage has a ripple profile as shown in Fig. 8.14.

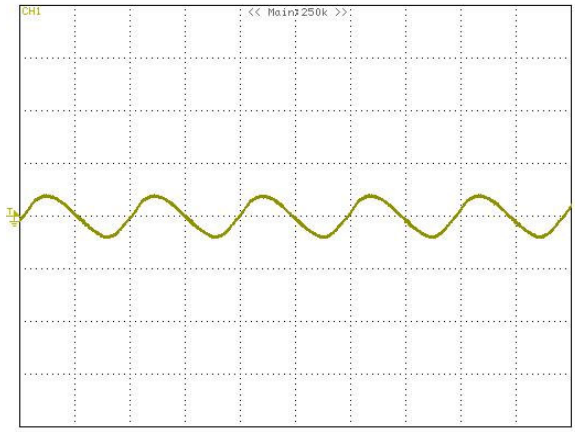


Fig. 8.14 Output Voltage Ripple (voltage scale: 0.2V/div, time scale: 5ms/div)

The output voltage exhibits 100Hz ripple component, this is due to imbalances on the input side transferred through the three converter modules, which result in the presence of a second harmonic component in the output voltage. The system was run under open loop control with the output voltage ripple measured for different load power levels. The results are shown in Fig. 8.15.

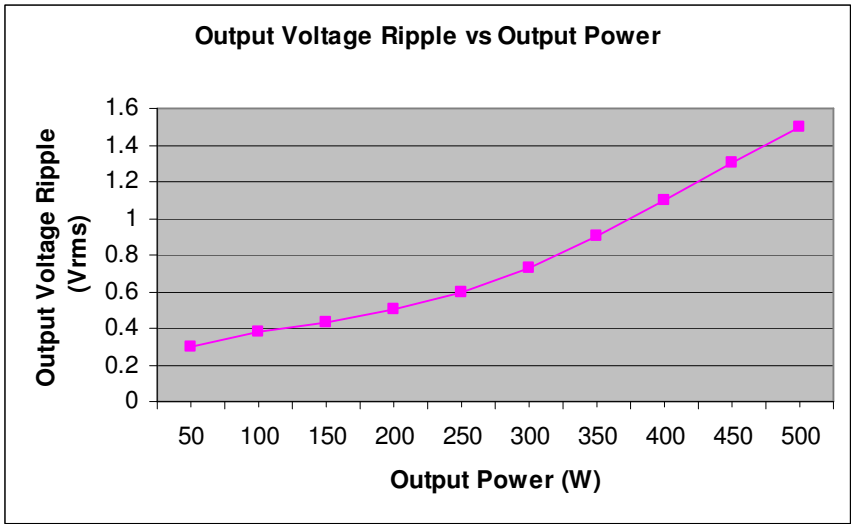


Fig. 8.15 Output Voltage Ripple vs Output Power

One can see the clear trend upwards for increasing power levels. This is expected, as more power is transferred to the load the greater the amount of voltage ripple will be present. It was found that at 500W the output voltage ripple was approximately 1.5Vrms. This can easily be improved by the addition of a multiple order tuned output filter. In [11] there is a discussion regarding the design of LC filters for ripple reduction with a three section LC filter shown to be able to provide 60db of attenuation. In order to reduce the voltage ripple from 1.5Vrms to 2mVrms (psophometric limit), requires 57.5db of attenuation, hence filtering alone would be able to reduce the ripple to acceptable limits. However, there is a weight issue in using passive filters with the necessary attenuation requiring 3.78kg of filtering [11]. Hence, the use of filtering in combination with dynamic power balancing as discussed in section 8.5, would help to reduce the ripple component

by providing power balancing between the individual converter modules. This in turn would reduce the filtering solution required and avoid incurring unnecessary costs in using heavy bulky passive components.

8.7 Phase Voltage Imbalance

In the "real world" mains voltage variations between phases is not entirely unexpected, as a result a feedforward loop has been designed to provide compensation against this phenomenon. A test was performed by introducing a 30% phase imbalance. This was carried out by applying an input voltage of 60Vrms on two phases and 48Vrms on the third phase. Fig. 8.16 shows the DSP compensating for the input imbalance by providing a 30% increase in the gain of the PWM controlling the converter module with the attenuated input phase voltage.

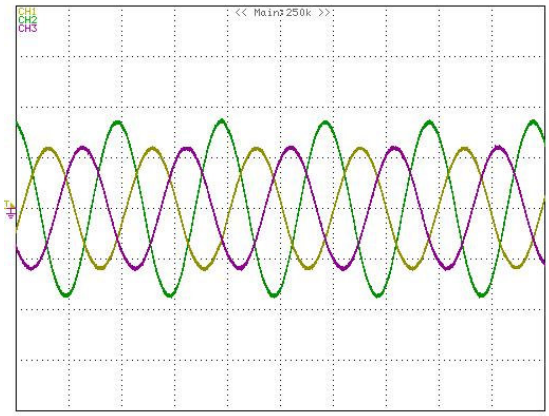


Fig. 8.16 PWM Output Waves (voltage scale: 0.5V/div, time scale: 5ms/div)

The output voltage ripple with and without feedforward compensation is shown in Fig. 8.17.

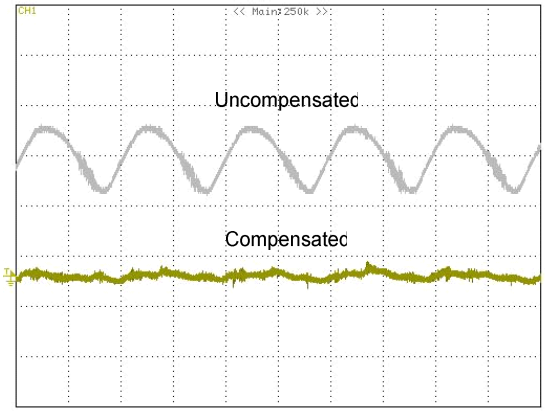


Fig. 8.17 Output Voltage (voltage scale: 1V/div, time scale: 5ms/div)

The feedforward control loop is able to compensate for the phase voltage imbalance by suppressing the large 100Hz ripple component. Thus, it is shown that the rectifier prototype is able to maintain a constant DC supply with reduced output voltage ripple even when operating outside its normal parameters. The output voltage ripple is not expected to comply with the psophometric standard under these conditions, since a system is tested against this standard only under steady-state conditions and with nominal mains voltages applied.

8.8 Converter Efficiency

The efficiency is examined in order to determine whether there is a clear advantage over existing two-stage topologies. Typical efficiencies reached by two-stage topologies are around 90%, with each stage having around 5% losses (i.e. 95% efficiency) [12]. The prototype is tested and the efficiency graph is shown in Fig. 8.18.

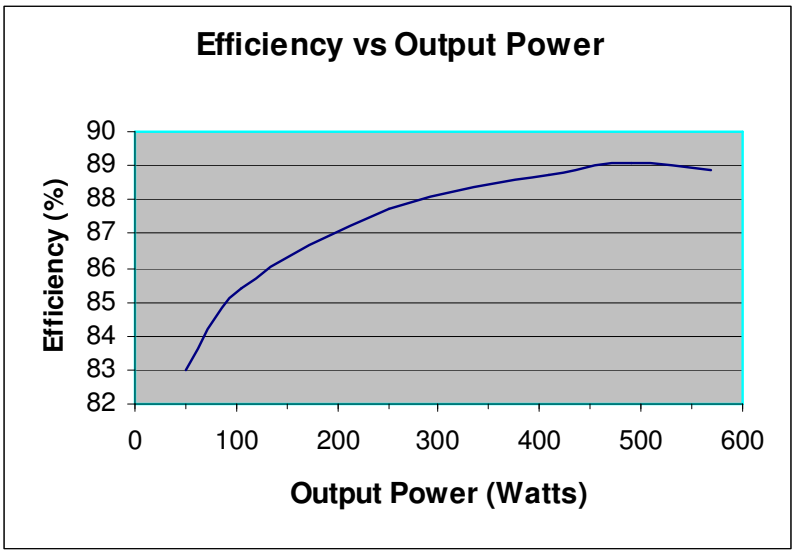


Fig. 8.18 Efficiency vs Output Power

The maximum efficiency of 89.3% occurs at 489W of output power. An efficiency audit was conducted to find out the distribution of losses.

The input diode bridge rectifiers used are a GBPC 3510W type with a 35A 1000V rating. At maximum efficiency an input current of 1.9Arms is drawn from each phase. There are two diode volt drops in each bridge rectifier at any one time giving a total of 6 diode drops in the system. According to the data sheet (see attached CD) the forward volt drop with 1.95A flowing is approximately 0.7V. The total losses for the diode bridge rectifiers are calculated as follows:

$$P_{BRIDGE} = 1.9A \times 0.7V \times 6$$

$$= 7.98 \text{ W}$$

The MOSFET losses are calculated, but since the system operates with zero voltage switching the losses are assumed to be conduction losses only. At any one time there are two MOSFETs switching in each converter module giving a total of 6 MOSFETs that are on in the power

converter system. The MOSFETs used are STW26NM60 devices with a rating of 26A and 600V. The conduction loss is an I^2R_{ds} loss, with R_{ds} being the drain source resistance. This resistance value is determined from the data sheet (see attached CD). Tests were carried out at a case temperature of around 25ºC as was confirmed by thermal measurements taken. The R_{ds} value was found to have a maximum value at this temperature of 0.135Ω from the data sheet. The rms current through the MOSFETs were measured and the total MOSFET power losses were calculated as follows:

$$P_{MOSFET} = (3.7A)^2 \times 0.135\Omega \times 6$$

$$= 11.9 \text{ W}$$

Transformer losses are calculated based on the assumption that each has around 99% efficiency, which is a standard expected value for a commercial quality transformer. Since each converter module carries a third of the output power which is 163W, the losses in each are expected to be 1.63W giving a total for the three of 4.89W.

The output chokes each carry half of the output power all of the time; hence the total power loss in the chokes also assuming 99% efficiency is 4.89W.

The output diode conduction losses are calculated by using the following formula:

$$P_{DIODE} = V_f \times I_{DC}$$

where V_f is the forward volt drop and I_{DC} is the current flowing through the diode. The forward volt drop for a given current is found from the data sheet in (see attached CD). The full output DC current flows through each of the output diodes in turn, hence the total conduction losses were found to be

$$P_{DIODE} = 1V \times 13A$$

$$= 13 \text{ W}$$

The output diode switching losses occur as a result of the fact that when the current decreases to zero, the diodes become reversed biased and must block twice the input voltage reflected through the transformer turns ratio. The output diode capacitance prevents the voltage from blocking immediately and instead, the resonant circuit formed by the inductance of the ZVS bridge converter modules and the diode output capacitance rings (see Fig. 8.19). In addition, due to the hard switching of the diodes, the reverse recovery current stores energy in the leakage inductance of the transformers, this can further exacerbate the ringing during diode turn off.

Snubbers are added to reduce the amount of ringing; however, the snubbers used are dissipative in nature made up of a series resistor and capacitor in parallel with the diode.

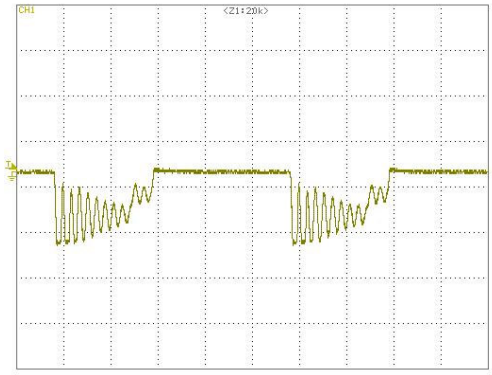


Fig. 8.19 Output Diode Ringing (voltage scale: 100V/div, time scale: 2μs/div)

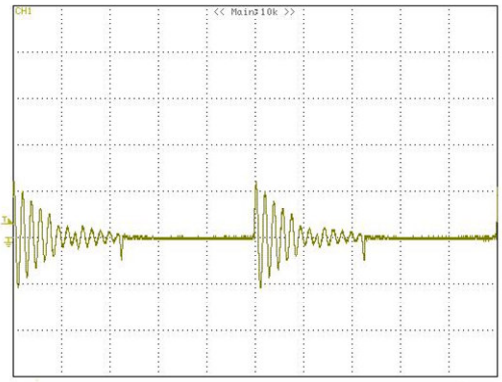


Fig. 8.20 Snubber Resistor Ringing (voltage scale:10V/div, time scale:2μs/div)

The snubber losses were calculated by measuring the following formula:

$P = \frac{V_{rms}^{\ 2}}{R} \times 6$ since there are 6 RC snubber circuits operating.

=6W

The input LC filter resistive losses were calculated based on the following formula:

$P_{FILTER} = I^2{}_{RMS} \times R \times 3$

$= (1.9A)^2 x(0.3\Omega)x3$

=3.2W

The distribution of losses is shown in table 2.

Bridge Rectifier	7.9W
MOSFETS	11.9W
Transformers	4.9W
Chokes	4.9W
Output Diodes	13W
Input Filter	3.2W
Snubber losses	6w
TOTAL	51.8W

Table 2 Loss distribution

The total 52.3W of losses in the system result in the 89.3% efficiency. Table 2 accounts for all but 0.5W of the losses. The majority of the losses are coming from the output diodes, as a result of the conduction losses due to the forward volt drop present. This loss can be reduced by replacement of the ultra fast diodes, with devices having a smaller forward volt drop at the same current levels. The MOSFETs constitute the second greatest loss as a result of having 6 of them being on at the same time. These losses are conduction losses since with ZVS there are no switching losses. The losses can be reduced by using MOSFETs with a lower R_{ds} values. These losses can be reduced firstly by using silicon schottky diodes which have reduced storage charge compared with ultra fast diodes and hence minimal reverse recovery. Secondly, the use of non-dissipative energy recycling techniques will further reduce the losses, the methods of implementation are discussed in [13-14], with [14] describing an efficiency gain of over 0.5%.

Since the majority of the losses are conduction losses, a simple replacement of the existing diodes (output and bridge), by those with lower forward volt drops, as well as with MOSFETs having low drain source resistance values, would result in an improvement in the overall efficiency.

8.9 Realisation

The prototype has its realisation requirements discussed and compared to the Vienna rectifier and the 6 switch buck converter introduced in chapter 3, as these are also single-stage isolated topologies. Discussions centre on the requirements for operation at 10kW.

The rectifier prototype requires three 700V rectifier modules for operation at 220Vrms mains voltages. The switching MOSFETs required 12 individual 600V components. The magnetics comprise three transformers and two output inductors which are required to each carry 100A which is half the output current. The output diodes consist of two 200V ultra fast diodes.

The Vienna 2 rectifier consists of three 800V rectifier modules and 5x500V MOSFETs. The diodes required on the input side are 6 lots of 600V components. The secondary rectification uses 4x60V Schottky diodes. The magnetics comprise 3 input boost chokes which are required to carry 3.3kW each and a single transformer to provide the isolation and voltage transformation.

The 6 switch buck converter consists of 6 AC switches rated at 1200V each. The output diodes are 600V soft recovery diodes. The magnetics consists of a transformer and an output choke which is required to carry the full output load current of approximately 200A.

8.10 Conclusion

This chapter has shown the operation of the three-phase power converter prototype, from the control circuit hardware layout, to the waveforms at various points in the system, giving an overview of the system operation. Various experimental results have been taken in order to demonstrate the operation and performance characteristics of the power converter prototype. The prototype topology is designed to enable ZVS to take place, the reason being to eliminate MOSFET switching losses. The ZVS operation of the system has been demonstrated, with results showing the ability to perform ZVS under light loads.

A PDF control strategy has been implemented with the results showing the strength of the control being its versatility in producing both a fast response to load step changes, as well as a slow response under startup conditions. Both the theory and results have shown that the PDF control strategy will naturally produce minimal overshoot during a load step change, and no overshoot during initial startup conditions, unlike the classic PI controller.

Further results have shown that the three-phase prototype power converter is able to comply comfortably with the IEC1000-3-2 standard, with recommendations for a control implementation which would further improve the current THD.

The output voltage ripple is larger than that required for compliance with the psophometric standard; however by implementation of power balancing control as well as the addition of output filtering, the output voltage ripple can be reduced to the required psophometric voltage level.

It has also been shown that the system is able to compensate for input voltage variations and so maintain an output voltage level with minimal ripple as a result of feedforward control. This feature

can be further extended to offer redundancy in the system, so that if one phase were to be lost, power can still be transferred via the remaining converter modules.

The maximum efficiency of the power converter was found to be 89.3%, with most of the losses as a result of the characteristics of the switching components. Further efficiency improvements are likely and methods have already been discussed in order to achieve this.

Also, a comparison is done between the prototype and two other three-phase converters namely the Vienna rectifier and the 6 switch buck converter. A comparison is undertaken regarding the realisation level required for each one.

Finally, recoding the DSP in assembler would result in reduced processing time and an improvement in the operating bandwidth. This would result in the prototype system being able to switch at 150kHz which would allow 220Vrms mains to be applied while operating under closed loop control.

8.11 REFERENCES

[1] J.M. Zhang, X.G. Xie, X.K. Wu and Z. Qian, "Comparison Study of Phase-Shifted Full Bridge ZVS Converters", IEEE Power Electronics Specialist Conference, Vol. 1, pp. 533-539, June 2004.

[2] H.N. Kutkut, "A Full Bridge Soft Switched Telecom Power Supply with a Current Doubler Rectifier", Telecommunications Energy Conference, pp. 344-351, Oct. 1997.

[3] V. Blasko, V. Vaura and W. Niewiadomski, "Sampling of Discontinuous Voltage and Current Signals in Electrical Drives: A System Approach", IEEE Transactions on Industrial Applications, Vol. 34, No. 5, pp. 1123-1130, Sept. 1998.

[4] S. Zheng and D. Czarkowski, "Modelling and Digital Control of a Phase-Controlled Series-Parallel Resonant Converter", IEEE Transactions on Industrial Electronics, Vol. 54, No. 2, pp. 707-715, April 2007.

[5] D.M. Mitchell, "Pulsewidth Modulator Phase Shift", IEEE Transactions on Aerospace Electronics, Vol. AES-16, No. 3, pp. 272-278 May 1980.

[6] T. Nussbaumer, M.L. Heldwein, G. Gong, S. Round, and J. Kolar, "Comparison of Prediction Techniques to Compensate Time Delays Caused by Digital Control of a Three-Phase Buck-Type PWM Rectifier System", IEEE Transactions on Industrial Electronics, Vol. 55, No. 2, Feb. 2008.

[7] D. Mattingly, "Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators", INTERSIL Technical Brief, Dec. 2003.

[8] Abraham Pressman, "Switching Power Supply Design", McGraw-Hill Inc., 1991.

[9] W.H. Lei and T.K. Man, "A General Approach for Optimizing Dynamic Response for Buck Converter", ON Semiconductor Application Note AND8143/D, April 2004.

[10] B.N. Singh, P. Jain and G. Joos, "Three-Phase AC/DC Regulated Power Supplies: A Comparative Evaluation of Different Topologies", Applied Power Electronics Conference and Exposition, Vol. 1, pp. 513-518, Feb. 2000.

[11] D.L. Loree and J.P. O'Loughlin, "Design Optimization of LC Filters", Power Modulator Symposium, pp. 137-140, June 2000.

[12] O. Garcia, J.A. Cobos, R. Prieto, P. Alou and J. Uceda, "Single Phase Power Factor Correction: A Survey", IEEE Transactions on Power Electronics, Vol. 18, No. 3, pp. 749-755 May 2003.

[13] H.M. Suryawanshi, M.R. Ramteke, K.L. Thakre and V.B. Borghate, "Unity-Power-Factor Operation of Three-Phase AC-DC Soft Switched Converter Based on Boost Active Clamp Topology in Modular Approach", IEEE Transactions on Power Electronics, Vol. 23, No. 1, pp. 229-236, Jan. 2008.

[14] R. Sheehy, J. Dekter and N. Machin, "Three Phase Power Factor Corrected Isolated Buck for 48V/100A", International Telecommunications Energy Conference, pp. 101-106, Oct. 2002.

9 DISCUSSION & CONCLUSION

9.1 Future Work

This thesis has presented a new rectifier concept prototype. The main idea for the development of the new topology was to provide an all-in-one system package that could provide the necessary characteristics to satisfy the various industry standards as well as giving an efficiency advantage and therefore a cost saving over the existing two-stage design. The theory behind the operation of the rectifier has been explained as well as the control strategy. There is still however scope for further work to be carried out in the optimisation of the feedback loop and the implementation of power balancing control schemes, in order to demonstrate the true ability of the PDF to provide highly responsive closed loop control.

There are also many opportunities for further research to be conducted in the area of analysing system design tradoffs. For example, scope exists for investigating the relationship between efficiency and cost.

The use of programmable logic in the form of FPGAs would open up possibilities in that switching frequencies would be able to be pushed higher to several hundred kilohertz thereby allowing the magnetics to be scaled down in size offering greater energy densities.

9.2 Original Contribution

The power converter topology is an original design concept with an international patent protection (IPN 350-00107-011). Further original contribution to the body of knowledge is through the structure of the three-phase PLL design. No other published work has been found to have previously used such an approach. Also, the PDF control strategy, although used in the area of motion control [1-4], no reference has been found to date using this type of control for switched mode power supplies.

9.3 Research Outcomes

During the course of the research documented in this thesis the following papers have been published. They appear in chronological order.

- W. Phipps, M. Harrison, & R. Duke, "New Generation Power Converter", Australian Universities Power Engineering Conference, Vol. 1, No. 12, pp. 363-368, Sept. 2005.

- W. Phipps, M. Harrison, & R. Duke, "Three-Phase Phase-Locked Loop Control of a New Generation Power Converter", IEEE Conference on Industrial Electronics and Applications, pp. 545-550, May 2006.

- W. Phipps, M. Harrison, & R. Duke, "A Novel Three-Phase Software Phase-Locked Loop", IEEE Conference on Power Electronics and Motion Control, pp. 172-177, Aug. 2006.

- W. Phipps, M. Harrison, & R. Duke, "A Proposal for a New Generation Power Converter with Pseudo-Derivative Control", IEEE Telecommunications Energy Conference, pp. 244-248, Sept. 2006.

- W. Phipps, M. Harrison, & R. Duke, "New Generation Power Converter", Australian Journal of Electrical and Electronic Engineering, Vol. 3, No.2, pp. 1-7, 2007.

- W. Phipps, M. Harrison, & R. Duke, "Phase Locked Loop Control of a Three-Phase Single-Stage Power Converter", Australian Journal of Electrical and Electronic Engineering, Vol. 4, No. 1, pp. 73-81, 2008.

9.4 Conclusion

The initial motivation in developing a new generation of rectifier topology was to see if it would be possible to have a topology that would yield a significant increase in efficiency over the traditional two-stage designs. It was identified that in order to achieve a cost reduction in the rectifier system, an increase the overall efficiency was needed. This would in turn give Eaton Power Quality Ltd. an advantage in the market place. The traditional two-stage converter designs resulted in a cascading effect of losses thereby reducing the efficiencies. It was therefore decided to investigate a new rectifier topology that would be a single-stage design, thereby theoretically netting an increase in overall efficiency while still been able to comply with the telecommunication industry standards. A new type of rectifier was developed for this purpose. The results showed that the rectifier was able to obtain around 89% efficiency, with traditional power converters having approximately 90% efficiency. It was identified that the majority of the losses were due to the conduction losses if the semiconductors. With the continued advancement of semiconductor technologies, such as CoolMos devices, which exhibit a lower on-resistance value compared with

standard MOSFETs. The new rectifier topology has the potential to exceed those efficiencies found in the traditional two-stage designs. Table 1 compares the different three-phase topologies as 10kW converters.

	6 switch buck	Vienna rectifier	Prototype rectifier
PFC	0.99	0.99	0.99
current THD %	<5	<5	12
control	complex	complex	simple
power (kW)	10	10	10
efficiency %	92	93	89
chokes	1	3	2
transformers	1	1	3
switches	6AC	5	12

Table 1 Comparison of Characteristics of Three-Phase Topologies

What is apparent with the new proposed rectifier compared with the other two is the poor current THD and lower efficiency. The control of the proposed rectifier is simple compared with the other topologies, however, in order for commercial realisation the current THD would need to be improved upon. Chapter 8.5 discusses a method of power balancing which could be used to improve on the current THD; however, employing this method would make the control more complex. The efficiency is relatively close to most of the other mentioned topologies, and thus using the suggested methods of improvement mentioned in chapter 8, it is expected that the efficiency of the proposed rectifier could sit somewhere in the 90-95% range.

Tests carried out showed that the converter is able to meet with all the required industry standards. The IEC1000-3-2 standard is comfortably met and suggestions for a further reduction in input current harmonics have been discussed. Although initial output voltage ripple results are above the psophometric noise limit the psophometric standard it has been shown that the standard can be

theoretically met with the addition of output filtering and feedback optimisation techniques having been described.

A PDF control strategy was tested with results showing excellent startup characteristics, having a smooth ramped response. This is a highly desirable feature which would reduce component stresses during the startup phase and thereby increase the life of the power converter (i.e. mean time between failures). The load step response is also improved with the PDF controller with a reduced overshoot resulting, when compared with that of a classic PI controller. The overall PDF response under load step changes could further be improved by the optimisation of the feedback loop.

The new generation rectifier has the advantage that it is able to provide constant DC output power during large input voltage imbalances, due to its ability to individually control the converter modules on each phase. This provides redundancy in the system, allowing power to be transferred to the load during mains phase aberrations.

A three-phase phase-locked loop structure has been introduced in this thesis with a detailed discussion found in chapter 5. This phase-locked loop topology has the advantage over the conventional three-phase topology in that no co-ordinate transformation is needed, thereby resulting in less digital processing time requirements, and hence a more efficient phase-locked loop.

Finally, although the new topology did not yield the immediate “quantum leap” in efficiency that was hoped for, it has shown to have the characteristics that would make it worthwhile to be taken from the prototype stage and be further developed into a successful commercial product.

9.5 REFERENCES

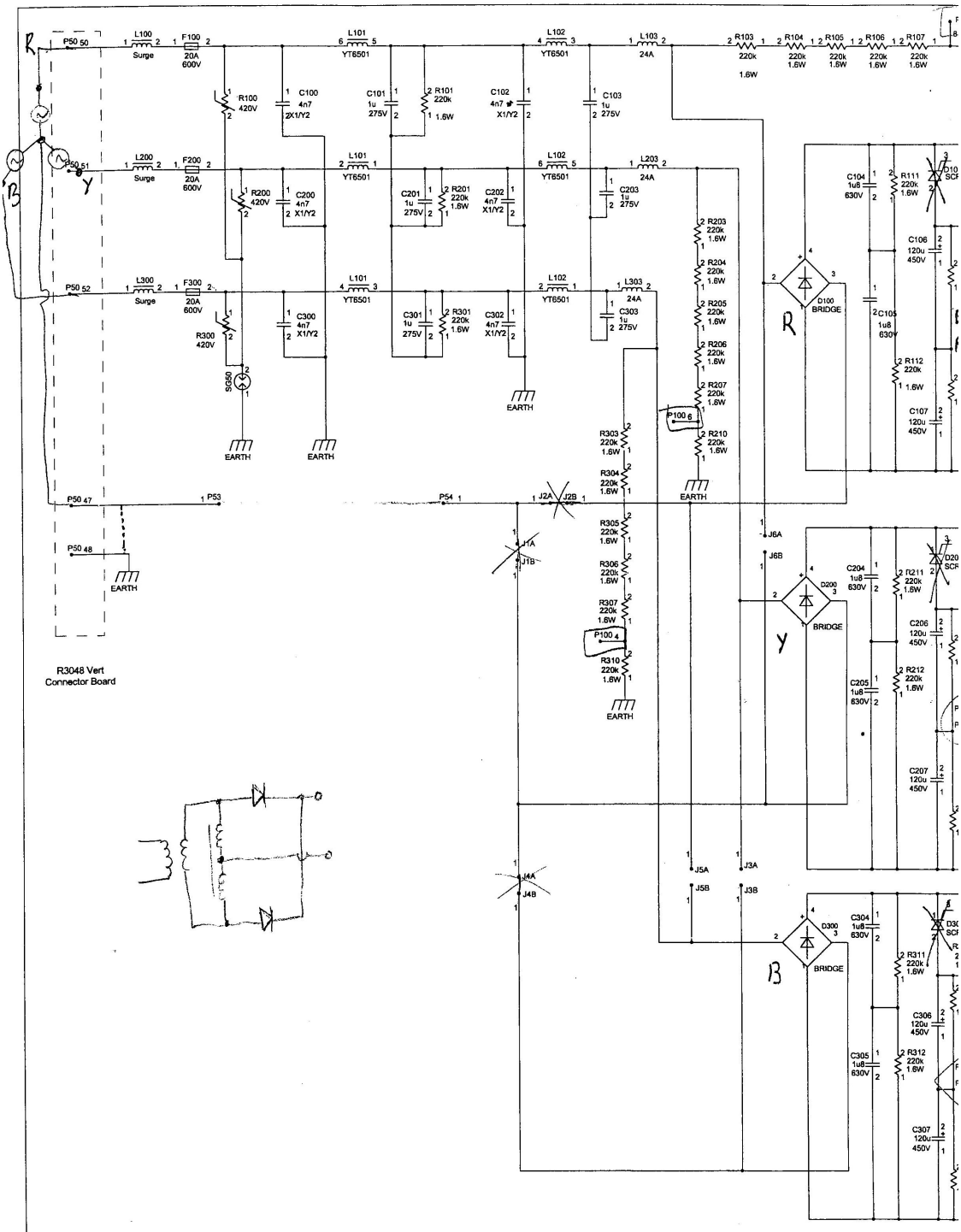
[1] J.K. Kang, J.T. Lee, Y. Kim, B. Kwon and K.S. Choi, "Speed Controller Design for Induction Motor Drives Using a PDF Control and Load Disturbance Observer", International Conference on Industrial Electronics, Control and Instrumentation, Vol. 1, pp. 799-803, Nov. 1991.

[2] P. Pillay and R. Krishnan, "Control Characteristics and Speed Controller Design for a High Performance Permanent Magnet Synchronous Motor Drive", IEEE Transactions on Power Electronics, Vol. 5, No. 2, pp. 152-159, April 1990.

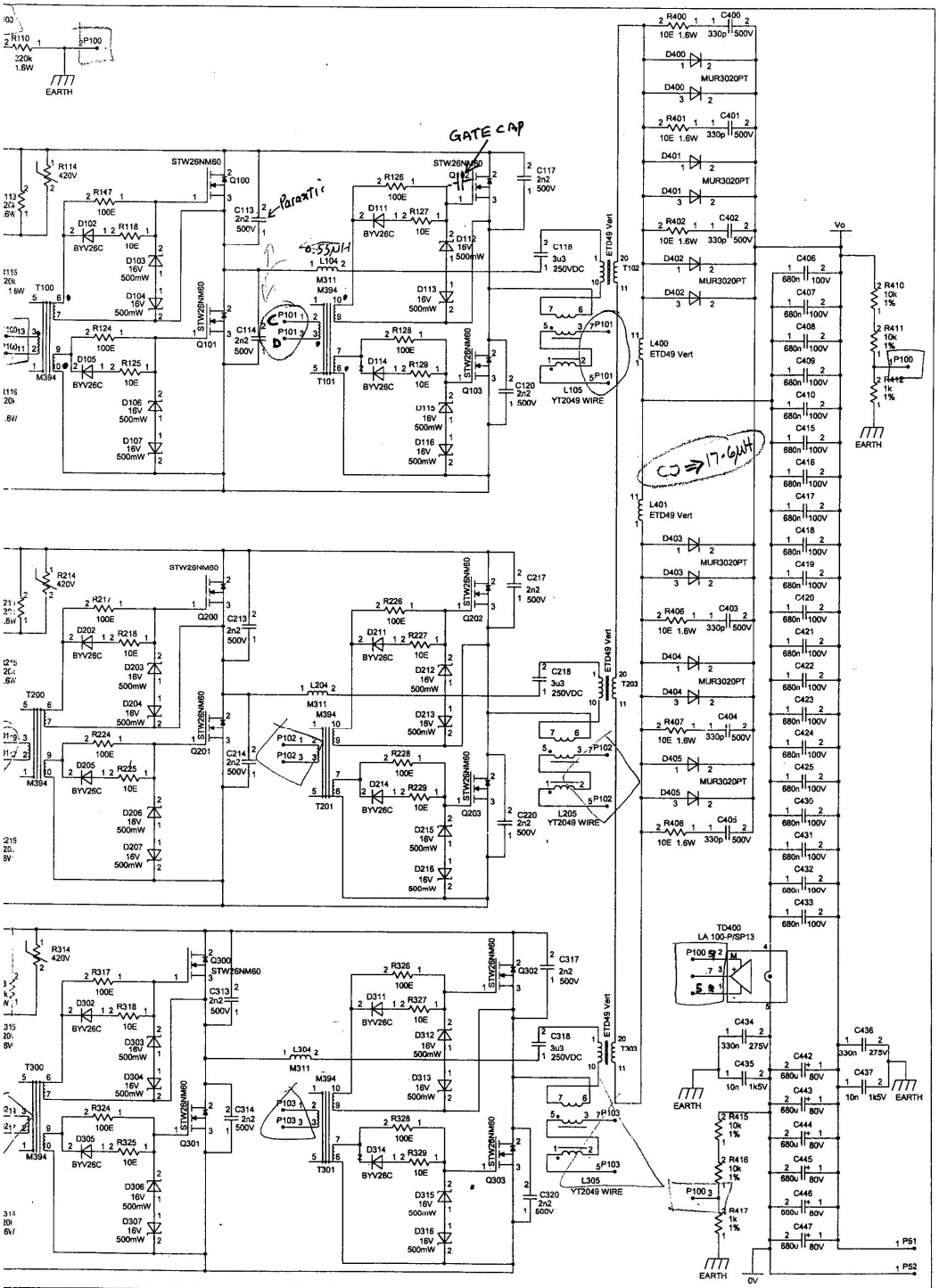
[3] M. Tang and L. Chen, "The System Bandwidth Analysis in Electro-Hydraulic Servo System with PDF Control", 5th Asian Control Conference, Vol. 3, pp. 1737-1745, July 2004.

[4] A. Vahedipour and J.P. Bobis, "Cascade Pseudo Derivative Feedback Control Algorithm and its Application to Design of Autopilots", International Conference on Industrial Electronics, Control and Instrumentation, Vol. 3, pp. 2368-2372, Nov. 1993.

APPENDIX A



ISSUE	AMENDMENTS	DRAWN	CHKD	APPD	DATE
1	PROTOTYPE 1	ANW			15.10.04



CIRCUIT DIAGRAM
NEW GENERATION 3 PHASE RECTIFIER

EATON CORPORATION, POWERWARE DIVISION

IPN

DRG 3679350

1 ISSUE

APPENDIX B

A Novel Three-Phase Software Phase-Locked Loop

William S. Phipps*, Richard M. Duke* and Michael J. Harrison†
* University of Canterbury, Department of Electrical and Computer Engineering, Christchurch, New Zealand
† Eaton Powerware, Christchurch, New Zealand

***Abstract*—This paper describes the development of a novel three-phase phase-locked loop (PLL) used to compensate for mains variations by being incorporated as part of a feedforward loop in a three-phase telecommunications power converter. A telecommunications converter must comply with industry standards, in particular the psophometric noise standard CCIF-1951; this is achieved by controlling the output voltage ripple from the dc-dc converter. It is required that psophometric compliance is maintained under expected mains variations documented in the EN50160 power quality standard. The software PLL is simulated and performance characteristics show a high degree of noise rejection while also maintaining good dynamic performance.**

I. Introduction

A new three-phase single-stage converter has been proposed [1]. These converters are manufactured for the telecommunications industry and as such need to conform to certain standards. The major ones are the CCIF-1951 standard, commonly called the psophometric standard, and the IEC1000-3-2 harmonic standard. The IEC1000-3-2 standard was introduced to regulate the harmonic currents drawn from the mains. Compliance with this standard is achieved by using active power factor correction techniques.

Telephone networks were originally analogue and because of output voltage ripple coming from the converter, audible noise was produced on the phone lines. Nowadays, with digital exchanges the telephone systems have become immune to dc power supply noise. The psophometric standard is still used however as the defining standard for the interface between telecommunication switching equipment and telecommunication dc power equipment.

This new design of converter achieves compliance by allowing constant three-phase power to flow from the source to the load by implementation of a squaring transfer function on the input voltages [1]. This action allows the load to be ripple free, as well as providing power factor correction. Given that the IEC1000-3-2 standard only needs to be met under nominal mains conditions, no further engineering effort is required with the design as compliance is virtually guaranteed. However, even under nominal operating conditions the psophometric standard will not be met due to the new converter design relying on the requirement that the three input phase voltages are balanced with equal magnitudes at all times in order to obtain zero output voltage ripple.

In order to theoretically maintain zero output voltage ripple a three-phase PLL is needed as a feedforward loop in order to compensate for mains variations between phases [1]. The PLL outputs serve as a reference; since it is synchronized with the mains, the outputs represent ideal mains voltages. Any discrepancies between the PLL outputs and the actual mains voltages then show up as an error signal that is fed forward with the converter controller generating the appropriate compensation signals used to maintain a constant power flow to the load. This prevents any voltage ripple due to mains amplitude variations from occurring [2].

A novel PLL design has been proposed in [2] and unlike the traditional three-phase PLL this new design involves no coordinate transformations, resulting in a more simple design that is computationally more efficient. Fig. 1 shows the PLL system.

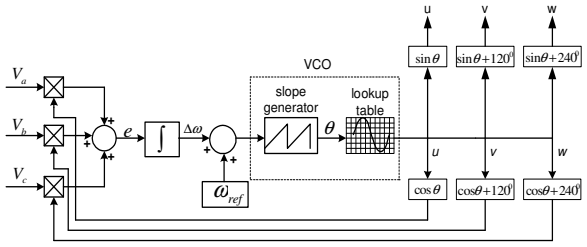


Fig. 1. Novel PLL Structure

It can be seen that the main difference between this new PLL compared with the traditional three-phase PLL is that there are no coordinate transformations and that the three phase detectors (multipliers), have their outputs summed together. This has the effect of cancelling the second harmonic signal, which is always present in single-phase PLL systems, as well as cancelling any common phase noise, thus reducing the overall filtering effort required [2]. Summing together the three phase detector outputs result in a dc error signal e. Elimination of the error signal is achieved by changing the phase of the feedback signals (u,v,w) to match the phase of the input voltages (V_a,V_b,V_c). The voltage-controlled oscillator (VCO) performs this task. If the error signal is zero the VCO produces a 50Hz quiescent frequency ω_{ref}, but if the error signal is a non zero value, then it responds by adjusting its operating frequency until a phase lock is achieved.

II. Software PLL Operation And Modelling

A. Operational Principle

The three-phase PLL software model is shown in Fig. 2.

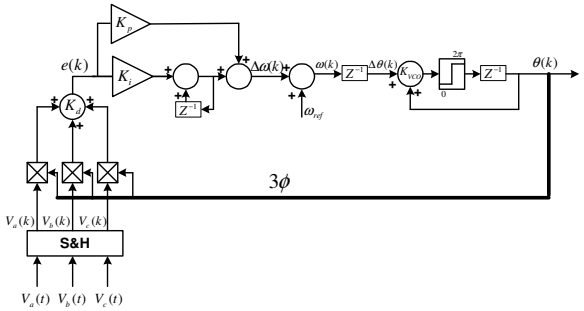


Fig. 2 Software PLL Model

The three-phase inputs after being sampled by the digital signal processor (DSP) are represented as

$$V_a(k) = 1PU\sin(\theta(k))$$
$$V_b(k) = 1PU\sin(\theta(k) + 2\pi/3)$$
$$V_c(k) = 1PU\sin(\theta(k) - 2\pi/3)$$

The multipliers serve as phase detectors, with the phase error in each phase being summed together resulting in a dc error signal *e(k)*. This error signal is fed into the proportional-integral controller of the PLL and used to calculate the change in angular frequency of the mains voltage $\Delta\omega(k)$.

$$\Delta\omega(k) = \left(K_p + \frac{K_i z}{z-1}\right)e(k)$$

The reference angular frequency $\omega_{ref}=2\pi f$ (where f is the reference frequency 50Hz), is added to $\Delta\omega(k)$.

$$\omega(k) = \Delta\omega(k) + \omega_{ref}$$

Multiplying $\omega(k)$ by the sampling time, which is represented by unit delay z^{-1}, determines the sampling time increment of the phase angle $\Delta\theta(k)$.

$$\Delta\theta(k) = z^{-1}\omega(k)$$

Integrating the increment $\Delta\theta(k)$ over the range 0-2π the estimated phase angle of each three-phase mains phase voltage $\theta(k)$ is obtained.

$$\theta(k) = \frac{z\Delta\theta(k)}{z-1}$$

The estimated angle is fed back into the phase detectors and used to adjust the error signal towards zero, resulting in the estimated angle and the grid phase angle being the same.

B. Modelling

By assuming the phase error is kept within a limited range, the PLL can be modelled as a linear system. This is a reasonable assumption since PLLs are normally only operated within their locking range, as beyond this range instability results [3]. A linear discrete model based on sampled data is shown in Fig. 3.

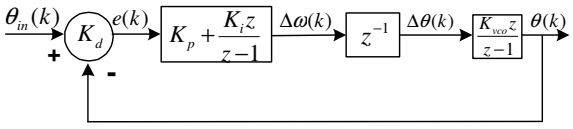


Fig. 3 Linear Discrete Software Model

In Fig. 3, as in Fig. 2, K_p and K_i represent the proportional and integral gains and z^{-1} represents a sample delay. In addition, K_d is the phase detector gain; it determines the phase detector output in response to a phase error. K_{vco} is the gain of the VCO. For equation simplicity we set $K_{vco}K_dK_p=\alpha$ and $K_{vco}K_dK_i=\beta$, and the closed loop transfer function of Fig. 3 can now be written as

$$\frac{\theta(z)}{\theta_{in}(z)} = \frac{(\alpha+\beta)z - \alpha}{z^2 + (\alpha+\beta-2)z + (1-\alpha)} \quad (1)$$

C. Loop Stability

A digital PLL is stable if all of its poles are inside the unit circle and unstable if any pole lies outside the unit circle. One of the most efficient criteria for testing the stability of a discrete-time system is Jury's stability criteria [3]. For a second order system, according to this criterion, the conditions for stability are

A(1)>0
A(-1)>0
$|k_0|<k_2$

where A is the denominator of the transfer function, which can be rewritten as

$A(z)=k_2 z^2+k_1 z+k_0=0$

applying these conditions stability is obtain when

$0<\alpha<2$ and $0<\beta<4$

D. Steady State Phase Error

Consider a step change in the phase of the incoming signal, which can be shown as

$$\theta_{in}(t) = u(t)\Delta\theta_{in}$$

$u(t)$ is the unit step function and $\Delta\theta_{in}$ is the size of the input phase step. The instantaneous phase has jumped from its old value to a new value by $\Delta\theta_{in}$. In the z domain this can be expressed as

$$\theta_{in}(z) = \frac{\Delta\theta_{in} \bullet z}{z-1}$$

and the phase error transfer function E(z) for a digital system can be expressed as

$$E(z) = \left[1 - \frac{\theta(z)}{\theta_{in}(z)}\right]\theta_{in}(z)$$

substituting (1) into E(z) gives

$$E(z) = \frac{\Delta\theta_{in} \bullet z(z-1)}{z^2 + (\alpha + \beta - 2)z + (1-\alpha)}$$

Applying the final value theorem to E(z)

$$\lim_{k\to\infty} e(kt) = \lim_{z\to 1} \frac{\Delta\theta_{in}(z-1)^2}{z^2 + (\alpha + \beta - 2)z + (1-\alpha)}$$

Setting z=1 it can be seen that the expression becomes zero, thus proving that the error signal over time will go to zero in response to a step phase change at the input. Further analysis shows similar results under conditions of a frequency step and a frequency ramp [4].

E. Coefficient Determination

To fully make use of the transfer function one needs to determine the relevant gain coefficients. The phase detector gain is the slope of the output calculated as cycles^{-1}. This was determined to be K_d=0.978cycles^{-1}. The VCO gain is the change in output frequency in response to an error signal, this was calculated to be K_{vco}=0.099cycles (see Appendix). To check the validity of these coefficients a cross check against expected values, based on the performance of the PLL, has been carried out. Setting K_p=0.0625 and given the following equation:

$$|\Delta f_l| = f_s K_{vco} K_d K_p \tag{2}$$

where f_s=sampling frequency and f_l=lock range

It was found that the lock range extended from 45Hz to 54Hz and since f_s=10kHz, Δf_l=9Hz and K_p=0.0625 the product $K_{vco}K_d$ was found to be 0.09 from (2). The same product, using analytical techniques described in the Appendix was found to have a value of 0.089. Therefore, these results give confidence that the calculated values are a fair reflection of the actual PLL internal system gains.

III. Performance Criteria

The desired performance of the PLL can now be implemented by adjusting the proportional and integral gains. A system that has a high bandwidth, although good for initial locking, does tend to enhance voltage distortions on the output [5]. Bandwidth is therefore a tradeoff between the filtering performance and the response time. The larger the bandwidth the better the response times, but the poorer the filtering action.

According to the European power quality standard EN50160, which provides the limits and tolerances of various phenomena that can occur on the mains, it is expected that the mains frequency may deviate by up to ±1Hz. Frequency can be represented as a change in phase angle over time given by the expression

$$\omega(t) = \frac{d\theta}{dt}$$

therefore, a ±1Hz grid frequency deviation is simply a change of 2π radians or 360˚ per second.

$$\frac{\Delta\theta}{\Delta t} = 2\pi$$

The required time for the mains to reach its steady state is now

$$\Delta t = \frac{\Delta\theta}{2\pi} \tag{3}$$

According to[6], dips in transmission services result in phase angle jumps of approximately ±5º or 5π/180. Substituting into (3), results in a settling time of 13.8ms.

The following time continuous approximations can be made for a digital system as discussed in [4].

$$\varsigma \approx \frac{1}{2}\sqrt{\frac{K}{K_i}} \tag{4}$$

$$\omega_n \approx f_s\sqrt{KK_i} \tag{5}$$

where

f_s= sampling frequency
K=loop gain= $K_dK_{vco}K_p$
ζ=damping factor
ω_n=natural frequency

The PLL is chosen to have a damping factor of 0.707 as this should allow only one overshoot in the transient response and it is well known to be the optimum damping factor value. Choosing values of K_p=1 and K_i=0.045 will give ζ=0.707 according to (4). Applying these values as well as the known values for K_{vco} and K_d to the transfer function in (1) gives the following closed loop transfer function:

$$H(z) = \frac{0.094z - 0.09}{z^2 - 1.906z + 0.91} \tag{6}$$

IV. Simulation

The transfer function in (6) has been simulated using a software package called PSIM. The input step response and the frequency and phase responses are shown in Figs. 4 and 5 respectively.

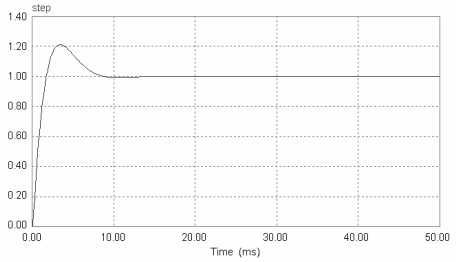


Fig. 4 PLL Input Step Response

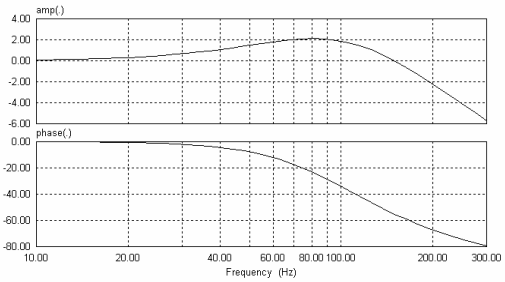


Fig. 5 PLL Frequency and Phase Response

From the simulations, it can be seen that the input step response (Fig. 4) yields a settling time of 8ms. The frequency response plot of gain (decibels) vs frequency (Hertz) (Fig. 5) shows that the PLL has a natural frequency of 149Hz, while (5) approximates to 121Hz. The phase response (Fig. 5) shows the phase angle (in degrees) vs frequency. The system is shown to have a phase margin of 126˚ and a gain crossover frequency of -54˚ indicating a stable system.

It can also be seen from the frequency response graph that there is some gain peaking. This is due to the fact that there is always a zero in the numerator of the transfer function even though the spacing between the zero and the closest pole decreases with increasing damping, but the pole never actually coincides with the zero therefore a second order PLL will always exhibit some peaking.

V. Software PLL Performance

A. PLL Experimental Setup

The proposed PLL technique is implemented using the DSP TMS320F2812. Some of the main features of this DSP are a 150MHz clock, analogue to digital converters (A/D) with 12-bit resolution and six PWM output ports [7]. Fig. 6 shows the experimental setup for the PLL. A three-phase function generator produces the mains voltages. The on-board A/D converters sample these input signals and consequently the PLL outputs the generated phase signals via the PWM ports. The outputs go through low pass filtering to remove the high frequency PWM switching harmonics.

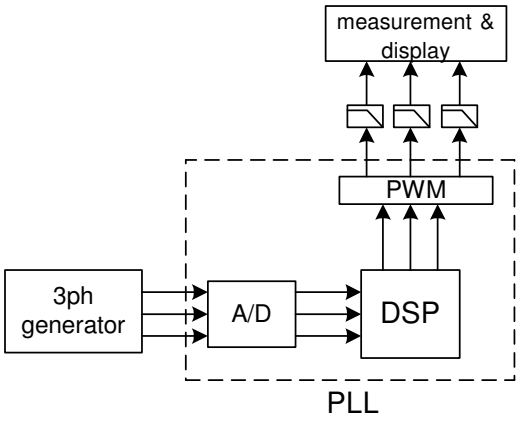


Fig. 6 Experimental Setup for PLL System

B. PLL Transient Response

The PLL is started up while the three-phase generated mains applied to the inputs and the response of the red phase is shown in Fig. 7. The PLL at startup has a 180˚ phase shift with respect to the input phase voltage and phase lock is achieved within 10ms.

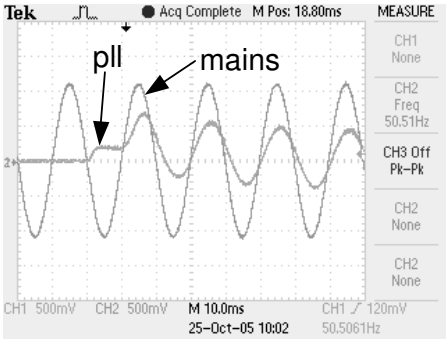


Fig. 7 PLL Startup Response

In Figs. 8 and 9, the PLL undergoes phase angle jumps. This is easier to perform than a phase jump on one phase of the function generator and yet achieves the same effective outcome of determining how well the PLL copes with a sudden phase angle change. A phase jump is achieved by resetting the VCO at the appropriate time. The response of the PLL to a phase angle jump of 90˚ is shown in Fig. 8 and it can be seen that the PLL is able to recover from the disturbance and regain tracking after 7ms. Fig. 9 shows that in the worst case, a 180˚ phase angle jump, the PLL regains synchronism in 10ms. The PLL output signals are generated by the PWM ports. Therefore, in order to see the output waveforms the PWM signals need to be filtered to remove the switching harmonics. As a consequence of passing the signals through a passive low pass filter, there is a phase shift introduced, hence the apparent phase shift between the mains and the PLL outputs.

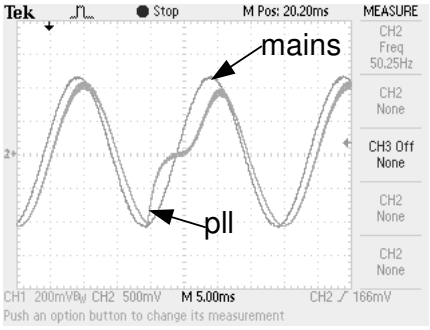


Fig. 8 PLL Under 90˚ Phase Angle Jump

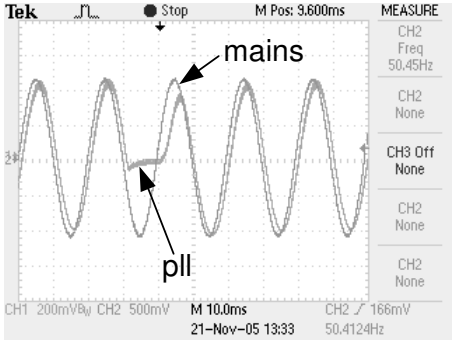


Fig. 9 PLL Under 180˚ Phase Angle Jump

C. *PLL Under Distorted Mains*

In reality the mains voltage is not a pure sinusoid but can be distorted by various non-linearity's such as phase imbalances and line harmonics.

In figures 10 and 11 the PLL output is shown under various three-phase mains distortions. The figures show a single phase input and corresponding output, however the waveforms are the same for all three phases.

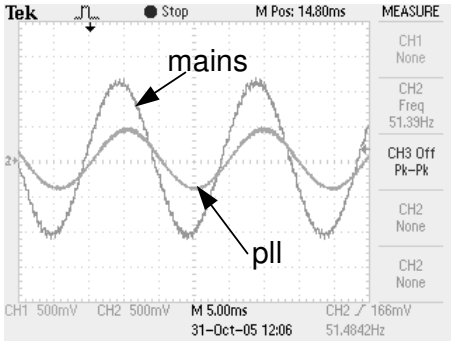


Fig. 10 Mains With Added Noise

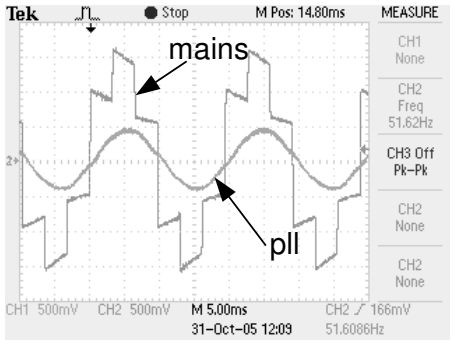


Fig. 11 Mains With Severe Harmonic Distortion

What can be seen from the waveforms is the ability of the PLL to maintain phase lock under distorted conditions. This is because the input phases are summed together resulting in a cancellation of all common phase distortions.

D. *Magnitude imbalance*

Introducing a phase imbalance, which can be seen in Fig. 12, a phase is attenuated by 10%, the expected maximum phase sag according to the EN50160 power quality standard. Applying this phase imbalance to the PLL results in the PLL obtaining phase lock, the results of one phase are shown in Fig. 13.

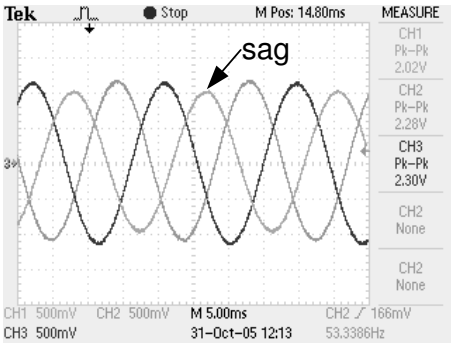


Fig. 12 Mains Phase Imbalance

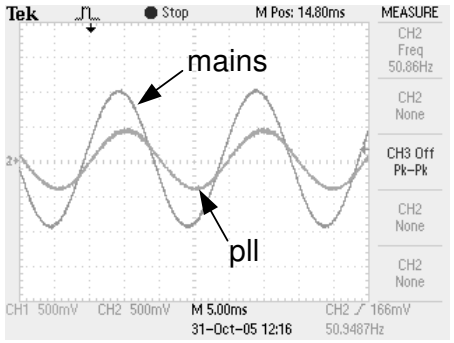


Fig. 13 PLL Output Under Phase Imbalance

VI. Conclusion

A novel software three-phase PLL has been introduced and a system model transfer function derived. Analysis has determined that for the particular application of the PLL used to monitor mains variations, the maximum required synchronisation time for the PLL after a phase angle disturbance is no more than 13.8ms.

Simulations of the transfer function transient response show a settling time of around 8ms with one overshoot. Simulations also show a natural frequency of 149Hz with a phase margin of 126˚ thereby indicating that the PLL is inherently stable.

The PLL was implemented on a DSP and the results show a worst-case 10ms synchronisation time in response to a phase angle jump. Under distorted mains conditions the PLL was shown to be able to maintain phase lock and produce a clean output waveform.

The PLL has been demonstrated to have a very good filtering action with the ability to naturally remove all common phase distortions; this allows the PLL system to have both excellent noise rejection and a high degree of robustness.

Acknowledgment

I would like to thank Eaton Powerware Ltd for their continued support for the converter project as well as the New Zealand Tertiary Education Commission.

References

[1] W. Phipps, M.J. Harrison, and R. Duke, "New generation power converter", *Australasian Universities Power Engineering Conference*, vol. 1, no. 12, pp. 363-368, September 2005.

[2] W. Phipps, M.J. Harrison, and R. Duke, "Three-phase phase-locked loop control of a new generation power converter", accepted for presentation at 1st IEEE Conference on Industrial Electronics and Applications, Singapore, May 2006.

[3] L. Xiu, W. Li, J. Meirs, and R. Padakanti, "A novel all-digital PLL with software adaptive filter", *IEEE Journal of Solid State Circuits*, vol. 39, no. 3, pp. 476-483, March 2004.

[4] F.M. Gardner, "Phaselock Techniques", 3rd ed., Wiley, NY, 2005.

[5] V. Kaura and V. Blasko "Operation of a phase locked loop system under distorted mains conditions", *IEEE Transactions On Industrial Applications*, vol. 33, no. 1, pp. 58-63, January 1997

[6] H. Awad, J. Svensson, and M.J. Bollen, "Tuning software phase-locked loop for series-connected converters", *IEEE Transactions On Power Delivery*, vol. 20,no. 1, pp.300-308, January 2005.

[7] TMS320F2812 data manual (Texas Instruments 2004).

Appendix

The phase detector gain K_d is determined by analysing the slope of the phase detector. The linear approximation of the phase detector is shown in Fig. 14.

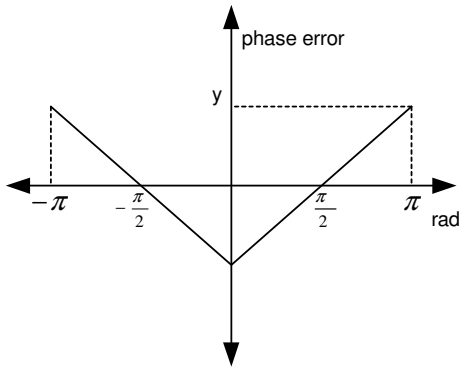


Fig. 14 Phase Detector Output

From empirical measurement y=24564 and the slope of the phase detector K_d is calculated as

$$K_d = \frac{24564}{\pi/2}$$

$$= 15638 rad^{-1}$$

Since the sampling frequency is 10kHz and the phase detector has the range $-\pi$ to π the number of cycles per radian is 15708. Therefore

$$K_d = \frac{15638}{15708}$$

$$= 0.978 cycles^{-1}$$

The VCO gain K_{vco} is calculated by determining the output of the VCO in response to an error signal.

The VCO concerned has a 0.063rad.s^{-1} change in frequency in response to the smallest error signal. Therefore

$$K_{vco} = \frac{0.063\, rad\, .s^{-1}}{10\, kHz}$$

$$= 6.3\times10^{-6}\, rad$$

Since the VCO generates a slope over the range 0-2π and with the sampling frequency of 10kHz, the VCO cycles are calculated as

$$= 6.3\times10^{-6}\, rad \times 15708\, cycles\, .rad^{-1}$$

$$= 0.099 cycles$$